Effects of High-K Dielectric with Metal Gate for Electrical Characteristics of Nanostructured NMOS

Norani Bte Atan, Ibrahim Bin Ahmad, Burhanuddin Bin Yeop Majlis and Izzati Binti Ahmad Fauzi

Abstract—This paper presents a systematic study of various high-K materials on metal gate MOSFET for 18nm NMOS. From this study, we find the suitable combination materials between the high-K and metal gate, and how it is a good affected on the electrical characteristics of 18nm NMOS. The device shows a good improvement on $I_{on}/I_{off}$ ratio, where the higher ratio that means this device it is suitable for low power applications. The virtually designed and fabricated of the devices was performed by using Athena module. While electrical characteristic performance was simulated by using Atlas module of SILVACO software. Physical properties such as high-K constant, low leakage current, threshold voltage and electrical characteristics were demonstrated. From the simulation result, it was shown that HfO2 is the best dielectric material with metal gate, TiSix.

Keywords—18 nm NMOS, High-K dielectric, Metal gate, Silvaco.

I. INTRODUCTION

New trend technologies, many industries have relied on a progression of smaller, denser, faster, cheaper and good quality of MOSFET. In order their main target is to reduce the production cost and at the same time can produce in big quantities of MOSFET. With increasing global competition, modern industries have to make their production process more efficient to compete. To do this, more advanced technologies have to be used. Scaling the MOSFET into nanometer regime, it is the best approach to solve many problems. It is a good and important challenging for future electronic technologies; refer to prospects of the scaling regime beyond 2011 ITRS [1].

Since MOSFET can be scaled down to smaller dimension which produce higher performance, at the same time gate length and oxide thickness also reduce. As the thickness scales of SiO2 below 2nm, leakage currents due to tunneling increase drastically, leading to high power consumption and reduce device reliability. Therefore, replacing the SiO2 with a high-K material allows increased gate capacitance [2]. The electrical characteristics of the device performance are analyzed with several of high-K materials and the gate oxide thickness is scaled to get same Equivalent Oxide Thickness (EOT). Recently, many researchers are focused on metal oxide materials with high-K values that have the ability to be integrated in MOSFET process flow. There are many high-K materials that are being studied nowadays such as Al2O3, HfO2, and TiO2 [3]. The best characteristics of gate dielectric should have high dielectric constant, large band gap with a favorable band alignment, low interface state density and good thermal stability. Among the high-K materials are compatible with silicon, and also materials have too low or high dielectric constant may not be adequate choice for alternative gate dielectric [4]. In this paper, we compare the electrical characteristics results for Titanium Silicide (TiSix) fabricated on Al2O3 (k~9), HfO2 (k~25) and TiO2 (k~85) gate dielectric. Thus the performance for all high-K materials with TiSix are explored and presented in the following section.

II. MATERIALS AND METHODS

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Between the channel regions, the deposition of high-K materials (Al₂O₃, HfO₂, and TiO₂) process with gate oxide thickness is scaled so that they have the same EOT with SiO₂ by analyzed electrical characteristics of the device. The length of the high-K material was scaled to get 18nm same as the gate length of transistor. Then, the implantation dose of boron on the N-well active area for the threshold voltage (V₉) adjustment process. Next, the Titanium Silicide (TiSix) deposited on the top of high-K materials (Al₂O₃, HfO₂, and TiO₂) and followed by halo implantation with adjusted of indium dose to obtain the optimum value of the NMOS device [7,8]. The next process was formation of the sidewall spacer. It used as a mask for source and drain implantation. In this case, implantation with arsenic dose and followed by phosphor dose respectively. It was to ensure the smooth current flow in NMOS device [9].

The next step was development 0.5 µm layer of Boron Phosphor Silicate Glass (BPSG). This layer acted as the Pre Metal Dielectric (PMD) [10]. Again, annealing process was done on the wafer to strengthen the structure under temperature 950°C. The last process of wafer was compensation implantation which using the phosphor dose. From the above experiment, the dosages quantities for boron, indium, arsenic, and phosphor were different which based on the high-K materials (HfO₂, TiO₂ and Al₂O₃). The last step was deposition of aluminum layer as the metal contact for source and drain. Therefore, under ATHENA module the design of 18nm NMOS structure already completed. There are many factors influence as the input process parameters on the threshold voltage 18nm NMOS such as Gate oxide thickness, Substrate implant dose, Pocket-halo implant tilt angle, Gate oxide diffusion temperature, V₉ implant dose, V₉ implant energy, Pocket-halo implant energy, Pocket-halo implant dose, S/D implant dose, S/D implant energy, Compensation implant dose and Compensation implant energy. Now, we will proceed the stimulation process under ATLAS module to measure the electrical characteristic such as I_D versus V_DS, I_D versus V_GS, I_on, I_off, and V₉.

III. RESULTS AND DISCUSSIONS

The complete fabrication of 18nm NMOS has been modeled and simulated successfully in Silvaco Simulink. Figure 1 shows the complete 18nm gate length NMOS. Figure 2 shows clearly on the doping profile of one of the design structure with gate length 18nm NMOS.

Results of electrical characteristic simulation are obtained in Figure 3 for I_D – V_DS and Figure 4 for I_D – V_GS with different materials of high-K such as Al₂O₃ (k~9), HfO₂ (k~25) and TiO₂ (k~85). Voltage, V_GS = 2.6 volts is applied for I_D – V_DS graph with different voltage of V_DS. While, V_DS = 1.4 volts is supplied for I_D – V_GS graph with different V_GS voltage. The threshold voltage (V₉), state on current (I_on) and state off current (I_off) can be extracted from I_D – V_GS curve.
A good doping concentration is one of the factors to ensure the transistor works well with fewer leakage current and enhance gate control [11]. There are four factors that influence in the threshold voltage countermeasure such as Threshold voltage adjustment implant, Halo implant, Channel implant, and Compensation implant. But for this research, only changing the various of dielectric material (Al₂O₃, HfO₂, and TiO₂) on the TiSix of transistor, so the Threshold voltage adjustment implant is best doping concentration to get a threshold voltage (VTH) 0.302651 with 6.03036 x 10¹³ cm⁻² boron for Al₂O₃. To maintain the same value of VTH, due to the physically thicker dielectric layer, therefore the boron doping for HfO₂ and TiO₂ were increased to 8.53256 x 10¹³ cm⁻² and 9.73654 x 10¹³ cm⁻² respectively. The increase of VTH adjustment implant doping concentration was proportional with increasing the value of high-K dielectric, and at the same time the values of drain current (Ion) were decreased as shown in Figure 5.

Drain leakage current (I_off) or sub-threshold leakage current occurs when the gate voltage (VGS) is lower than the threshold voltage (VTH). In ideal case, when the transistor is turned off, VGS = 0 volt and VDS = VDD (voltage supply), there is no current can through into the channel (I_off = 0). Refer to Figure 6, the leakage current for HfO₂ dielectric is lowest compared with Al₂O₃ and TiO₂ dielectrics. It is means, HfO₂ dielectric material most compatible with silicon and most stable oxide with the highest heat of formation [12,13].
Figure 7 shows the $I_{on}/I_{off}$ current for different materials of high-K dielectric. HfO$_2$ dielectric gives the highest $I_{on}/I_{off}$ ratio compared with Al$_2$O$_3$ and TiO$_2$ dielectrics. Hence, better performance of device can be obtained by using HfO$_2$ dielectric as gate oxide. This device is suitable for low power application [14].

Table 1 shows the simulated results for different materials of high-K dielectric with ITRS 2011 prediction. The highest $I_{on}/I_{off}$ ratio is obtained with HfO$_2$. Therefore, all the above high-K materials are suitable with metal gate and compatible with silicon of transistor. The best choice is HfO$_2$ as dielectric of transistor.

### Table 1. Simulated Results of Various Dielectric materials With ITRS 2011 Prediction

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Al$_2$O$_3$</th>
<th>HfO$_2$</th>
<th>TiO$_2$</th>
<th>ITRS 2011 Prediction</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{TH}$(V)</td>
<td>0.302651</td>
<td>0.302651</td>
<td>0.302651</td>
<td>0.302</td>
</tr>
<tr>
<td>$I_{on}$</td>
<td>4.7212x10$^{-4}$</td>
<td>2.5355x10$^{-4}$</td>
<td>1.9336x10$^{-4}$</td>
<td>1.0x10$^7$</td>
</tr>
<tr>
<td>$I_{off}$</td>
<td>2.3652x10$^{-15}$</td>
<td>1.9123x10$^{-16}$</td>
<td>2.4316x10$^{-14}$</td>
<td>1.496x10$^4$</td>
</tr>
<tr>
<td>$I_{on}/I_{off}$ ratio</td>
<td>1.9961x10$^{17}$</td>
<td>1.3259x10$^{12}$</td>
<td>7.9519x10$^9$</td>
<td>6.6845x10$^7$</td>
</tr>
</tbody>
</table>

Table 1 shows the simulated results for Al$_2$O$_3$, HfO$_2$ and TiO$_2$ dielectric materials with TiSix as metal gate for 18nm NMOS. $I_{on}$ results from the simulation are bigger value compared prediction value. While the simulation results for $I_{off}$ are lower than prediction value. Therefore, all the above high-K materials are suitable with metal gate and compatible with silicon of transistor. The best choice is HfO$_2$ as dielectric of transistor.

### IV. Conclusion

NMOS structure with 18nm were successfully designed and simulated to study the various of dielectric materials on metal gate of device performance. The performance of the three dielectric materials, Al$_2$O$_3$, HfO$_2$ and TiO$_2$ with TiSix as metal gate were compared and it was found HfO$_2$ is the best dielectric material for the future nano scale MOS devices technology. It based on the highest value of $I_{on}/I_{off}$ ratio, and lowest value of sub-threshold leakage current ($I_{off}$). It is suitable for low power application.

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