An Efficient Hybrid Voltage/Current mode Signaling Scheme for On-Chip Interconnects

M. Kavicharan, N.S. Murthy, and N. Bheema Rao

Abstract—Conventional voltage and current mode signaling schemes are unable to meet the speed requirements and power specifications in deep submicron technologies. The challenges posed by aggressive interconnect scaling forces VLSI circuit designers to look for alternative signaling techniques at nanometre technology nodes. Voltage mode signaling is very slow while current mode signaling suffers from serious static power dissipation problem. This paper presents a novel hybrid voltage/current mode VLSI interconnect signaling scheme which addresses the above problems. In which, both the proposed interconnect driver and receiver circuits are controlled by an efficient Schmitt trigger based control circuit which generates control signals based on input data transitions. These circuits switch from voltage mode to current mode for high data rates as a result of smaller voltage mode schemes for the data rates more than 90 Mbps. It is also observed from the simulation results that the power dissipation and the power delay product (minimum energy) of the proposed scheme are much better than those of voltage and current mode schemes for data rates of >20 Mbps.

Keywords—Current mode, Delay, Hybrid mode, Power, Power delay product, Schmitt trigger, Voltage mode, VLSI Interconnect.

I. INTRODUCTION

As the technologies are scaling down, the performance of on-chip global interconnects has become a bottleneck in modern VLSI chips. The conventional signaling schemes [1]-[4] such as voltage-mode are not able to meet the speed requirements and power specifications of future technology generations. Hence, these specifications force designers to look for alternative signaling techniques for addressing interconnects scaling problems. Voltage mode with repeaters insertion scheme for driving long interconnects was a popular scheme to reduce delay, but increases significant power dissipation in VLSI circuits. The delay dependence on the line length changes from quadratic to linear [1], but power dissipated by repeater circuits increases linearly with line length [5]. With aggressive interconnect down scaling, line length increases leading to more number of repeaters which further increases the power dissipation. As an alternative to voltage mode signaling with repeaters, current-mode signaling was developed and validated for SRAM circuits [6]-[8]. Later current mode scheme was improved by [9]-[13] for better performance.

The conventional current mode scheme signal propagation can be up to three times faster than voltage mode scheme [14]. The significant reduction of delay in current mode signaling is due to loading of the line with low impedance receiver which shifts the system dominant pole [15]. In general, an important advantage of current mode signaling over voltage mode signaling is that, its dynamic power dissipation component can be significantly reduced as a result of smaller voltage swings in the interconnect [3]. However, the major drawback with conventional current mode scheme is the static power consumption at low data rates. Hence, current mode scheme is generally suitable only for long buses carrying high activity data.

In ideal voltage mode signaling, driver drives an open circuited interconnect, which causes the output to follow input. In the case of current mode signaling, load is a short circuited interconnect (ideally zero) and hence there exists a continuous current path. This leads to static power dissipation, which limits its use in short interconnects or low data rates, hence voltage mode is better at lower data rates [16]. In addition, it has also been observed that [17], current mode signaling consumes even more power than voltage mode with repeaters. This is the motivation to develop a novel hybrid voltage/current mode circuit which offers the advantages of both voltage mode and current mode for low and high data rates respectively. Repeater less signaling over 10nm line using the proposed hybrid scheme is presented in this paper, which is the major difference from another hybrid scheme [18].

This paper presents an adaptive bandwidth approach using a hybrid voltage/current mode circuit which operates in current mode for high input data rates otherwise in voltage mode with much reduction in static power dissipation. The performance of the proposed hybrid scheme is compared with voltage mode...
and current mode circuits in terms of 50% delay and power consumption. Another important metric for design of all electronic circuits is power delay product, which indicates the degree of energy dissipation in a circuit. Hence, power delay product as a figure of merit should have minimum value for good design. It has been found that, out of existing voltage and current mode schemes, the proposed hybrid scheme has better power delay product for input data rates of above 20 Mbps.

The rest of the paper is organised as follows. Section 2 presents a brief discussion on voltage and current mode interconnects in an attempt to clear the basic idea of various modes. In section 3, the proposed hybrid voltage/current-mode scheme is discussed along with Schmitt trigger based control circuit. Section 4 compares the performance of proposed scheme with current mode scheme and voltage mode schemes. Conclusions are drawn in section 5.

II. VOLTAGE MODE VS CURRENT MODE

The generalised distributed RLC model of voltage/current mode interconnect is shown in Fig.1. The unit length Resistance, Capacitance and Inductance are represented as R, C and L respectively, and dl is denoted as length of each lumped section. The driver is modelled as an inverter with an output capacitance of Cs and receiver is approximated as a parallel combination of R L and C L respectively. Input signal V_in employs random input data of Non-return-to-zero (NRZ) format.

According to signaling point of view, both voltage and current-mode driver circuits are similar and drive distributed model of RLC interconnect. On the other hand, current mode receiver offers low impedance load while voltage mode receiver provides a high impedance capacitive termination [15]. Fig.1 shows that, for a voltage mode receiver of load capacitance C_L, addition of a parallel low impedance resistance R_L will change its operation to current mode.

III. HYBRID VOLTAGE/CURRENT MODE SCHEME

The block diagram of the proposed hybrid voltage/current-mode scheme for global interconnects is shown in Fig.2. It consists of driver and receiver circuits with input and control signals. The necessary control signals are generated by Schmitt trigger based control circuit. The same control signals should be given to both the driver and receiver circuits with proper timing synchronization. The driver and receiver circuits operate in two modes (voltage-mode and current-mode) based on control signals (V_cnt, V_cntb). If the control signals are V_cnt =1 and V_cntb =0 the circuit operates in current-mode for high data rates otherwise in voltage-mode for low data rates.

A. Control signal generation circuit

Fig.3 shows schematic of control signal generation circuit, which generates control signals (V_cnt and V_cntb) based on input data transitions. The circuit consists of an inverter based charge pump and a Schmitt trigger [19]. The conventional Schmitt Trigger complete design is presented by Filanovsky and Baltes [20]. The circuit is designed such that for higher input data rates the control signal V_cnt is high and for slowly varying signals control signal V_cnt is low, depending on the duration of the input pulse width.

If the voltage across capacitor is zero, transistors M5 and M6 are OFF and M3 and M7 are in linear mode of operation hence, the control voltage V_cnt = V_dd. When the capacitor voltage rises above V_cnt, M6 becomes ON and M8 source node voltage starts decreasing, it causes M5 to be ON and control
voltage starts decreasing. For fast data activity, the capacitor does not have enough time to charge/discharge hence, the capacitor voltage remains below threshold voltage $V_{tn}$, leading to $V_{cnt} = V_{dd}$. Similarly for slow variation of input data activity, the capacitor voltage and feedback transistors ensure $V_{cnt}$ to be below $V_{tn}$. Thus, for small variation in input data activity the control voltage $V_{cnt}$ signal is low otherwise high.

Control voltage must be high before the high frequency input signals are applied such that current mode operation (low impedance load) can be invoked at the driver and receiver circuits without delay. In the absence of input data transitions or low data rate signals control voltage $V_{cnt}$ can be automatically discharged to low such that power dissipation is minimized in voltage mode operation. The charging time of control signal defines the setup time which ensures the input data signal transitions must be stable before the stable state of control voltage.

C. Hybrid voltage/current-Mode Receiver Circuit

The hybrid voltage/current-mode receiver circuit is shown in Fig. 5, consists of a voltage mode receiver, diode connected M22 and M23 transistors followed by a low gain amplifier (an inverter with gain $A \approx 25$). The receiver operates in voltage mode and current mode depending on $V_{cnt}=0$ and 1 respectively. In voltage mode the receiver operates in full swing mode whereas in current mode the receiver input voltage swings around the switching threshold of the diode connected inverter. The inverter acts as a low gain amplifier and will generate full swing voltage levels at the output.

IV. SIMULATION RESULTS

The operation of the proposed hybrid voltage/current mode scheme was simulated in 180nm CMOS technology for $V_{dd}$ of 1.8V. The presented schemes were designed for the line length of 10mm with typical line dimensions using predictive technology model (PTM) [21] of 180nm technology. The per unit length interconnect parameters were extracted using the field solver TCAD Raphael and are presented as follows: $R=42.5 \Omega/cm$, $L=2.311 \text{nH/cm}$, $C=17.43 \text{pF/cm}$, $G=0.443 S/cm$ and $R_s=0.00135 \Omega/cm$. The simulation results of voltage mode, current mode [23] and proposed hybrid voltage/current mode are obtained using HSPICE W-element method. As per 1999.4 release of HSPICE, at high frequency operation the imaginary term of the skin effect has been added for accurate frequency response.

The frequency dependent resistance including skin effect is given by

$$R(f) = R + R_s(1+j\sqrt{f})$$

where $R$ is the DC resistance and $R_s$ is the skin effect resistance.

B. Hybrid voltage/current-Mode Driver Circuit

Fig. 4 Hybrid voltage/current-mode Driver circuit

Fig. 5 Hybrid voltage/current-Mode Receiver circuit

For higher data rates when $V_{cnt}$ is high, activates the right half of the driver circuit and operates in current-mode with low swing (Fig. 7). This causes the dynamic power dissipation of current mode operation to be lower than voltage mode full swing operation. When $V_{cnt}$ is high, M13 NMOS gives weak high and M16 PMOS gives weak low. Hence, the voltage swing on the wire can be reduced. Depending on the control signals, input data can be transmitted either through left half voltage mode driver or right half current mode driver.
Table 1. Performance comparison @20 Mbps (wire length=10 mm) of various schemes

<table>
<thead>
<tr>
<th>Scheme</th>
<th>Delay (ns)</th>
<th>Power (µW)</th>
<th>Power Delay product(ns-µW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage-Mode</td>
<td>1.283</td>
<td>7.13</td>
<td>9.14</td>
</tr>
<tr>
<td>Voltage-Mode with Repeaters [22]</td>
<td>1.069</td>
<td>16.45</td>
<td>17.58</td>
</tr>
<tr>
<td>Current-Mode [23]</td>
<td>0.296</td>
<td>140.35</td>
<td>41.54</td>
</tr>
<tr>
<td>Proposed hybrid scheme</td>
<td>1.317</td>
<td>7.259</td>
<td>9.56</td>
</tr>
</tbody>
</table>

Table 1 shows the performance comparison between the various schemes for 10 mm line at low data rate of 20 Mbps. In this case hybrid voltage/current mode scheme switches to voltage mode scheme at low data rates and hence the advantage of zero static power is utilised. As compared to other schemes the delay and power dissipation of proposed scheme are approaching voltage mode scheme. The power delay product of the proposed hybrid voltage/current scheme is much less than the voltage mode scheme with repeaters [22], current mode scheme [23] and almost equal to simple voltage mode scheme.

Table 2. Performance comparison @400 Mbps (wire length=10 mm) of various schemes

<table>
<thead>
<tr>
<th>Scheme</th>
<th>Delay (ns)</th>
<th>Power (µW)</th>
<th>Power Delay product(ns-µW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage mode</td>
<td>1.283</td>
<td>144.4</td>
<td>185.26</td>
</tr>
<tr>
<td>Voltage mode with repeaters [22]</td>
<td>1.069</td>
<td>181.2</td>
<td>193.7</td>
</tr>
<tr>
<td>Current mode [23]</td>
<td>0.296</td>
<td>190.2</td>
<td>56.29</td>
</tr>
<tr>
<td>Proposed hybrid scheme</td>
<td>0.502</td>
<td>80.29</td>
<td>40.3</td>
</tr>
</tbody>
</table>

Table 2 shows the performance comparison between the various schemes for 10mm line at high input data rate of 400 Mbps. In this case hybrid voltage/current mode scheme switches to current mode and hence the advantage of high speed operation is utilized at high data rate. Increasing the data rate to 400 Mbps yields better improvements in relative performance for the proposed scheme approximately 2.5 times decrease in delay over the voltage mode scheme [1] and approximately half of the power is saved when compared with the above schemes. Furthermore, the power delay product as a figure of merit is much better when compared with other schemes.

Fig. 6 Simulated waveforms of input signal, control signal, Receiver input signal and Output signal of voltage mode interconnect operation when control voltage=0.

Fig. 6 shows an input data stream (V_{in}), control voltage (V_{cnt}), voltage mode driver output and the output data of proposed scheme. As stated earlier, for slow input data activities the control voltage V_{cnt} is set as low and operates in voltage mode. The proposed scheme operates in voltage mode and the driver output is having large swing which is in contrast with the current mode driver output small swing, as shown in Fig. 7.

Fig. 7 Simulated waveforms of input signal, Control voltage, Driver output and Output signal of current mode interconnect operation when control voltage=1.

Fig. 7 shows an input data stream (V_{in}), control voltage (V_{cnt}), current mode driver output and the output data of proposed scheme. For high data rates of input, the output of control signal V_{cnt} is set as high and operates in current mode. From the Fig. 7 it is clear that, the driver output voltage of current mode scheme has low swing of 0.2 V when compared with voltage mode driver output full swing of 1.8 V results in lower delay.
The proposed hybrid voltage/current-mode scheme combines the benefits of voltage-mode and current-mode techniques. The circuit switches to voltage mode or current mode based on the control signal which is input data dependent. At lower data rates the circuit operates in voltage-mode scheme whereas it switches to current-mode scheme for higher data rates, thus it includes the advantages of both voltage mode (zero static power consumption) and current mode (for high speed operation). At data rate of 400 Mbps, the proposed scheme has approximately 2.5 times decrease in delay over the voltage mode scheme and approximately half of the power is saved when compared with the presented schemes. For the data rates of >20 Mbps, the proposed hybrid voltage/current mode circuit power delay product is better than the existing schemes. The proposed scheme also provides an alternative solution for the placement-constrained repeater inserted wires.

V. CONCLUSIONS

The proposed hybrid voltage/current-mode scheme combines the benefits of voltage-mode and current-mode techniques. The circuit switches to voltage mode or current mode based on the control signal which is input data dependent. At lower data rates the circuit operates in voltage-mode scheme whereas it switches to current-mode scheme for higher data rates, thus it includes the advantages of both voltage mode (zero static power consumption) and current mode (for high speed operation). At data rate of 400 Mbps, the proposed scheme has approximately 2.5 times decrease in delay over the voltage mode scheme and approximately half of the power is saved when compared with the presented schemes. For the data rates of >20 Mbps, the proposed hybrid voltage/current mode circuit power delay product is better than the existing schemes. The proposed scheme also provides an alternative solution for the placement-constrained repeater inserted wires.

REFERENCES


