VLSI Implementation of an improved multiplier for FFT Computation in Biomedical Applications

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***Abstract*—Discrete Fourier Transform (DFT) is a fundamental Digital Signal Processing domain transformation technique used in many applications for frequency analysis and frequency domain processing. Fast Fourier Transform (FFT) is used for signal processing applications. It consists of addition and multiplication operations, whose speed improvement will enhance the accuracy and performance of FFT computation for any application. It is an algorithm to compute Discrete Fourier Transform (DFT) and its inverse. DFT is obtained by decomposing a sequence of values into components of different frequencies. FFT can compute DFT in O(N log N) operations unlike DFT computation that takes O(N2) arithmetic operations . This reduces computation time by several orders of magnitude and the improvement is roughly proportional to N / log N. Present day Research focus is on performance improvement in computation of FFT specific to field of application. Many performance improvement studies are in progress to implement efficient FFT computation through better performing multipliers and adders.**

Electroencephalographic (EEG) signals are invariably used for clinical diagnosis and conventional cognitive neuroscience. This work intends to contribute to a faster method of computation of FFT for analysis of EEG signals to classify Autistic data.

Keywords—FFT, Multiplier, EEG

I. INTRODUCTION

Modern applications are demanding high speed computations. Technology is coming close to theoretical limits on how fast computations can be done on a single chip. Multiple processors operating in parallel, performing different functions of a process and combining them at the end is the solution to this. Fourier Transform is the basis of many signal processing and communication applications. It is the tool for analysis of the signal in its frequency domain. Fourier transform has many applications, in fact any field of physical science that uses varying signals, such as engineering, physics, applied mathematics, and chemistry, will make use of Fourier series and Fourier transforms. Most of these fields nowadays make use of digital and discrete data. Thus the determination of Fourier Transform of discrete signals is of prime importance and such a transform is called Discrete Fourier Transform (DFT). Fast Fourier Transform (FFT) is an efficient algorithm to evaluate DFT.

Discrete Fourier Transform has a wide range of applications. It is mainly used for converting discrete time domain signals to its frequency domain. However, the process of conversion is expensive and takes lot of time. Thus we go for Fast Fourier Transform which uses a divide-and-conquer approach to reduce computational complexity of DFT. DFT is defined as

$$X(k) = \sum_{n=0}^{N-1} x(n).W_N^{nK} \qquad (1)$$

where n,k ϵ [0,N-1] and $W_N^K = e^{-j2\Pi k/N}$ is the twiddle factor, x(n) is the nth sample of discrete time signal and X(k) is its frequency sample at kth instant.

Complexity of computation of DFT is O (N^2) unlike the computation of FFT which is O (N log N) butterfly operations. Hence DFT computation takes more time and is a costlier process. FFT algorithm deals with these complexities by exploiting regularities in the DFT algorithm. Radix-2 Algorithm is a common factor algorithm for N-point DFTs, where N is a power of 2. FFT computation in Radix-2 system takes place in $\log_2 N$ different steps, hence it enables pipelining in hardware design.

FFT computation involves addition and multiplication operations. As multipliers are slow performing hardware units, their performance directly affects the performance of the FFT hardware. Existing hardware multipliers are Serial Multiplier, Array Multiplier, Booth Multiplier, Wallace Tree Multiplier, Booth encoded Wallace tree multiplier, etc. Studies on performance optimizations of Booth Multiplier, Wallace Tree Multiplier and Booth encoded Wallace Tree Multipliers are in progress. Improvement in terms of Hardware Description Language (HDL), Floor planning, Routing, etc. are of main interest to Researchers. This work intends to compare the performance of main hardware multipliers and study and implement the most efficient multiplier for FFT computations in biomedical field.

FFTs are extensively used in data compressions, filtering signals, Signal spectral analysis, Image Processing, etc. In

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Biomedical field, Medical Imaging plays an important role for diagnostics of various health conditions. Electroencephalography (EEG) and electrocardiography (ECG) are various techniques to study the patterns of signals generated by brain and heart, respectively. These are further researched to clinically study human behaviour and heart functions. This work analyses spectral components of EEG signals and proposes an effective method to classify EEG levels of Autistic children.

II. Fast Fourier Transform Algorithm

Fast Fourier Transform is an algorithm to compute Discrete Fourier Transform which diminishes the number of computations for n-point radix from N^2 to N logN arithmetic operations. There are two methods to compute DFT through FFT algorithm, namely, Decimation-in-time (DIT) and Decimation-in-frequency (DIF) FFT algorithms. In Radix-2 DIT-FFT, input signal is decimated into even-indexed and odd-indexed values such that the series x(n) where, n=0, 1,2,…N changes to x(2r) and x(2r+1) where r=0,1,2,….N/2-1. In Radix-2 DIF-FFT, the x(n) series is broken into x(n) for n=0,1,2….N/2 -1 and x(n) for n=N/2, N/2+1,….N-1.

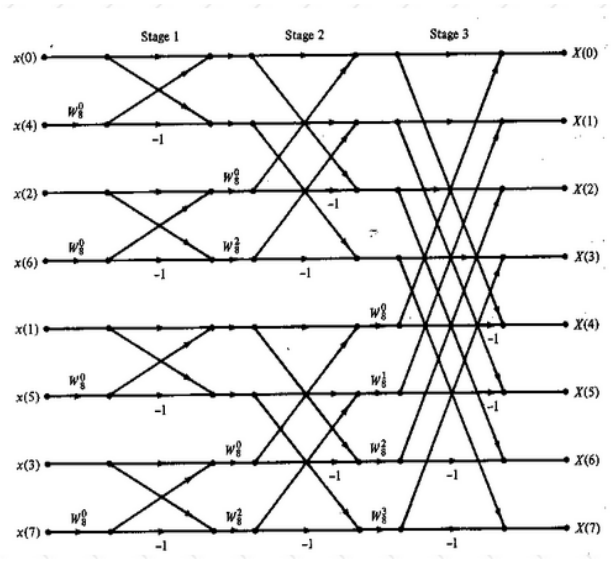

Fig. 1. Radix-2 8-point DIT-FFT algorithm

Fig. 1 shows the butterfly structure of an 8-point Radix-2 DIT-FFT algorithm. Eight time-domain inputs, namely, x0, x1, x2, x3, x4, x5, x6, x7 are transformed to their frequency components, namely, X0, X1, X2, X3, X4, X5, X6 and X7 in three stages. This paper implements Radix-2 8-point DIT-FFT algorithm.

III. Multipliers

Multipliers have large area, long propagation delays and consume power. Therefore, low-power multiplier design has an important role in design of low-power VLSI systems. Power refers to number of Joules dissipated over a certain amount of time whereas energy is the measure of the total number of Joules dissipated by a circuit [9]. In digital CMOS design, the well-known power-area/power-delay product is commonly used to assess the merits of designs [9].

Any multiplier design involves 3 steps. They are i) partial product generation ii) partial product reduction and addition iii) final addition. The partial products are formed first either by using an algorithm or using AND gate for each bit of the multiplier with each bit of the multiplicand. The next step is reduction of these partial products. The third step is addition of the remaining partial products to yield the final product [9].

Hardware multipliers widely used are Booth Multipliers and Wallace Tree Multiplier. Area and Power parameters of Booth Multiplier and Wallace Tree Multiplier are studied and their advantages have been incorporated to develop the concept of Booth-encoded Wallace Tree Multiplication.

A. Booth Multiplier

Booth Multiplier implements Booth Algorithm, named after its originator, A. D. Booth. This algorithm is implemented for signed multiplication of integers and can be extended to real numbers. Algorithm is based on recording the multiplier to a recorded value leaving the multiplicand unchanged [6] i.e.

• Each ‘0’ digit is retained in the recorded number until 1 is encountered on evaluating from LSB to MSB.

• Complement of 1 is inserted at every ‘1’ digit in recorded number and all other succeeding 1’s are complemented until a ‘0’ is encountered.

• Then, replace the ‘0’ with ‘1’ and continue the process.

Two main drawbacks of Booth Algorithm are the inefficiency of the circuit when isolated 1’s are encountered and difficulty in designing parallel multipliers as number of shift-and-add operations may vary. Hence Modified Booth Algorithm was developed by O. L. Macsorley. Modified Booth Algorithm is twice as fast as normal Booth Algorithm [4]. This modified Booth Encoding algorithm reduces the number of partial product rows to (N +2)/2 where N is the number of bits of Multiplier or Multiplicand [4].

B. Wallace Tree Multiplier

Wallace Tree Multiplier is one of the hardware multipliers used to accomplish high speed and low power multiplication to condense the number of partial products generated. There are two main techniques followed in designing Wallace Tree Multiplier. First technique is to consider all bits in each column at a time and compress them into two bits, namely, Sum and Carry. Second technique is to consider all bits in four rows at a time and compress them. Wallace Tree Multipliers use half adders, full adders, 4:2 and 3:2 compressors and a high speed adder [10].

Partial product generation, partial product addition and final addition are the three stages in a multiplier. In Wallace Tree Multiplier, the multiplicand is multiplied by the multiplier, bit-by-bit, to generate partial products. They are, then, added based on Wallace Tree structure to produce two rows of partial products which are finally added using any high speed adder. The critical path delay of Wallace Tree multiplier is

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proportional to the logarithm of the number of bits in the multiplier [9].

Algorithm for Multiplication of two signed integers is as follows:

• Multiply (AND) each bit of one of the arguments,

• Reduce the number of partial products to two by layers of full adders and half adders (Compressors).

• Group the wires in two numbers, and add them with a conventional adder [9].

Wallace tree multiplication can be implemented only for signed integers and are avoided for low power applications as excess wiring consumes more power.

C. Booth-Encoded Wallace Tree Multiplier

Based on the comparative study of Area and Power parameters of Booth Multiplier and Wallace Tree Multiplier, Booth-encoded Wallace Tree Multiplier is chosen as an efficient multiplier for FFT computation. Table I. shows Area and Power performance parameters of the two multipliers which are coded in Verilog HDL and performance parameters are evaluated using IC Compiler tool from Synopsys Inc. Though Wallace Tree multiplier shows better performance in terms of Area and Power than Booth multiplier, its operation is limited to signed integers alone. As FFT computation in biomedical applications involve signed real numbers, Booth Algorithm is to be implemented for the multiplier.

TABLE I. PERFORMANCE PARAMETERS OF 4X4 BOOTH MULTIPLIER AND WALLACE TREE MULTIPLIER

Multiplier	Area(nm^2)	Power(µW)
Booth Multiplier	974.872	235.184
Wallace Tree Multiplier	600.868	180.504

Multiplication of the two operands, Multiplicand (MD) and Multiplier (MR) results in 2N bits for conventional multiplication. However, Booth encoded multiplier reduces number of partial products to (MD/2 -1) partial products [5]. Booth Algorithm is based on recording the multiplier to a recorded value leaving the multiplicand unchanged. It scans the multiplier operand and skips chains. It reduces the number of additions required to produce the result [4]. Booth-encoded Wallace Tree Multiplier has advantages of both Booth Multiplier and Wallace Tree Multiplier. This paper implements Booth encoding to increase speed of algebra by reducing number of partial products and Wallace Tree module for decreasing number of levels of addition.

1) Architecture of the Multiplier

In Booth encoded multiplier, number of partial products are reduced by grouping multiplier bits into pairs and selecting partial products from the set {0, M, 2M, 3M} where M is the multiplicand. Modified Booth encoded multiplier, avoids the use of Carry Propagate Adder to calculate 3M, rather it utilizes Carry-Save-Adder. Thus, in Modified Booth Algorithm, number of partial products is reduced by a factor of two without a pre-adder to produce partial products [6]. Multiplier decoding is done such that multiples needed are in {0, M, 2M, 4M + -M} data set. These multiples can be generated using shift-and-complement methods.

Fig.2 shows the architecture of Booth-encoded Wallace Tree Multiplier which consists of five blocks, namely, 2's Complement Generator, Booth Encoder, Partial Product Generator, Wallace Tree module and Carry Look-ahead Adder [7]. Booth encoder inspects each bit of the multiplicand and records the multiplier in terms of 0, 1 and complement of 1. As complement of 1 cannot be represented on hardware, operational equivalent of recorded multiplier is implemented based on Table II. Here, outputs of the encoder. x and z are defined as:

$$x = MR[i] \bullet MR[i-1] \quad (2)$$

$$z = MR[i] \oplus MR[i-1] \quad (3)$$

Where MR[i] and MR [i-1] corresponds to i^{th} and $i\text{-}1^{th}$ bit of Multiplier, respectively. 2's complement generator takes the multiplicand MD as input and produces –MD as output .i.e. inverts all bits of multiplicand and uses a Ripple Carry Adder to generate 2's complement. Partial product generator generates appropriate partial products to be added in Wallace tree structure. Wallace Tree module adds all partial products. Addition is implemented using Carry Look Ahead Adder [7].

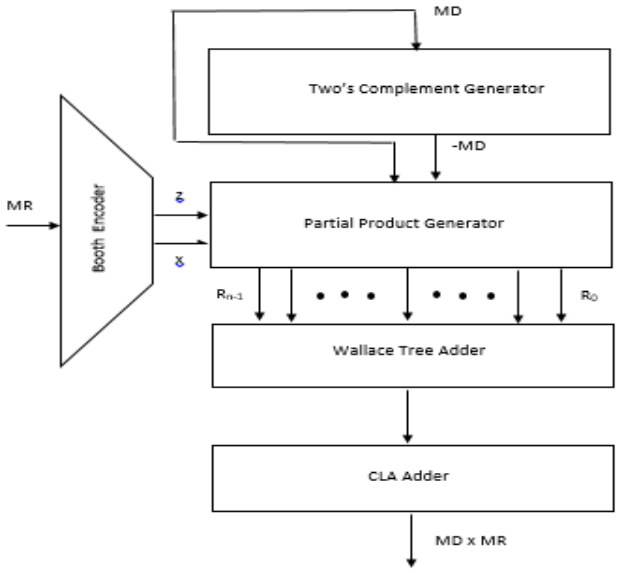

Fig. 2. Booth-encoded Wallace Tree Multiplier

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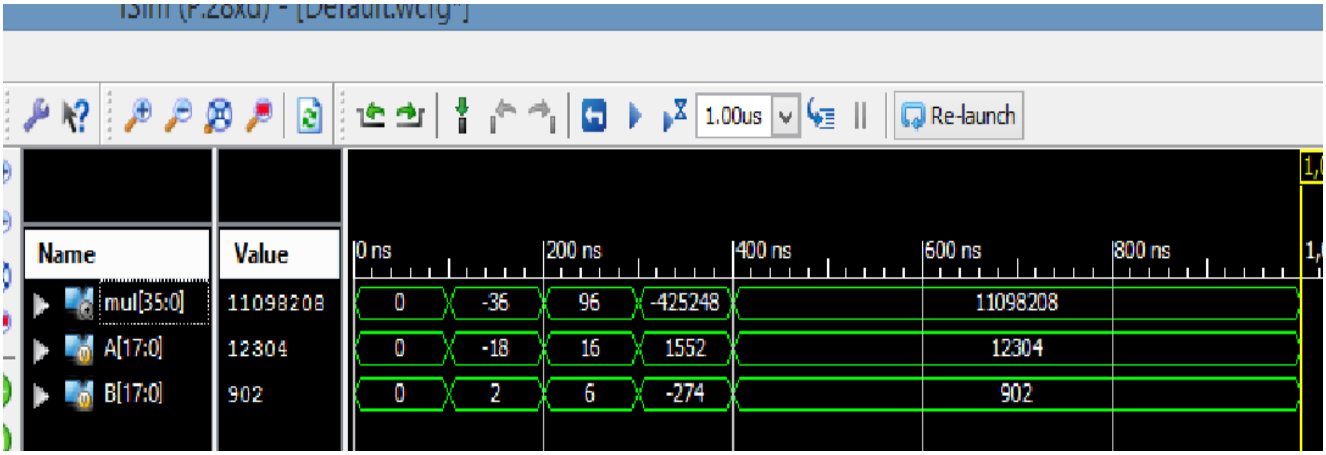

Fig. 3. Simulation Results of Booth-encoded Wallace Tree Multiplier

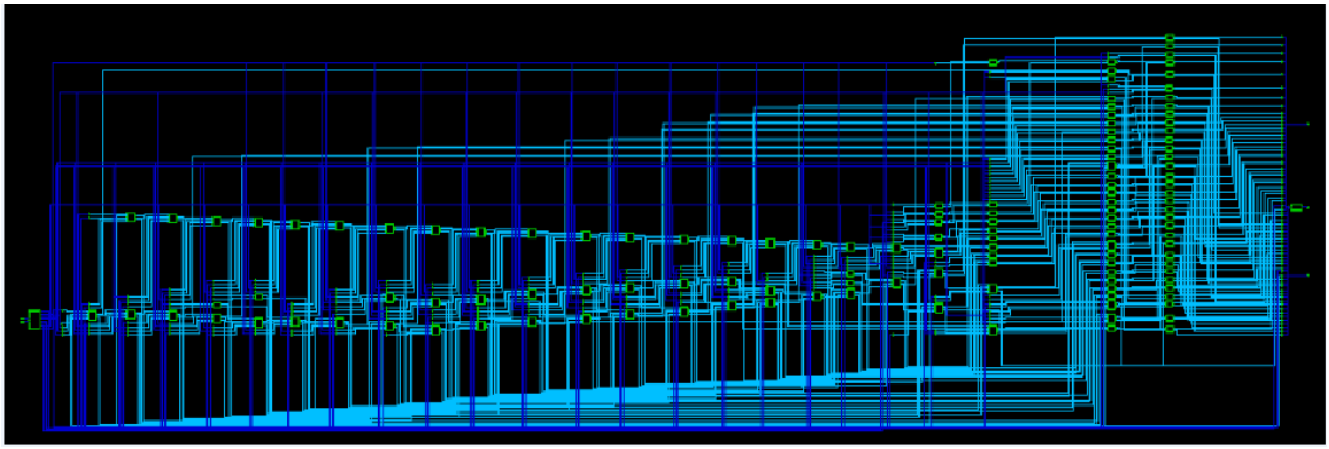

Fig. 4. Generic Gate-level Schematic of Booth-encoded Wallace Tree Multiplier

TABLE II. BOOTH ENCODING VALUES

MR[i]	MR[i-1]	Recorded y[i]	x	z	Assigned to partial product
0	0	0	0	0	0
0	1	1	0	1	MD. sign extended
1	0	$\bar{1}$	1	1	-MD, sign extended
1	1	0	0	0	0

Hardware Description Language (HDL) implementation of Booth-encoded Wallace Tree Multiplier has been done in Verilog HDL. The outputs are correctly obtained for both signed and unsigned multiplication. Simulation has been done using Xilinx ISE tool. Generic Gate-level schematic has been obtained in IC Compiler tool from Synopsys Inc. Fig. 3 and Fig. 4 show the simulation results and Generic Gate-level Schematic of the Booth-encoded Wallace Tree Multiplier.

IV. FFT WITH BOOTH-ENCODED WALLACE TREE MULTIPLIER

FFT implementation using Booth-encoded Wallace Tree Multiplier is an efficient circuit with advantages of both Booth Multiplier and Wallace Tree Multiplier. As explained in II, Modified Booth Algorithm is used to calculate Partial Products as per Table II. Partial Product Generator provides minimum number of partial products which are added using Wallace Tree structure. Hence, efficient algorithm of multiplication is implemented.

Radix-2 8-point DIT-FFT has been coded in Verilog HDL for input values scaled up by a factor of 10000. There are ten inputs to the circuit, namely, eight time-domain samples, Twiddle factor 'wr' and the scaling factor 'k'. Outputs are separately obtained for real and imaginary parts of corresponding frequency components.

As 8-point corresponds to 3 stages ($8 = 2^3$), twiddle factor varies for each stage. Twiddle factor is calculated as in (1). For N=1, Twiddle factor value is {1}, for N=2, Twiddle factor values are {1, -j} and for N=3, Twiddle factor values are {1, -j, $(1/\sqrt{2}) - j(1/\sqrt{2})$, $(-1/\sqrt{2}) - j(1/\sqrt{2})$}. Depending on the accuracy of outputs required, scaling can be varied from 10 to any power of 10 and by increasing the number of significant digits of twiddle factor value of $(1/\sqrt{2})$. Simulation results shown in Fig.5 has been scaled up for a factor of k = 10000. Outputs and inputs have been correctly verified. Accuracy of $\pm 0.1\%$ is obtained for scaling improvement from 1000 to 10000.

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Design Vision tool from Synopsys Inc. is a logic synthesis tool which inputs HDL design and synthesize out gate-level HDL net lists. Fig. 6 shows the Generic Gate-level schematic diagram implemented in 90 nanometer technology using saed90nm_typ_ht.db library in IC Compiler tool from Synopsys Inc.

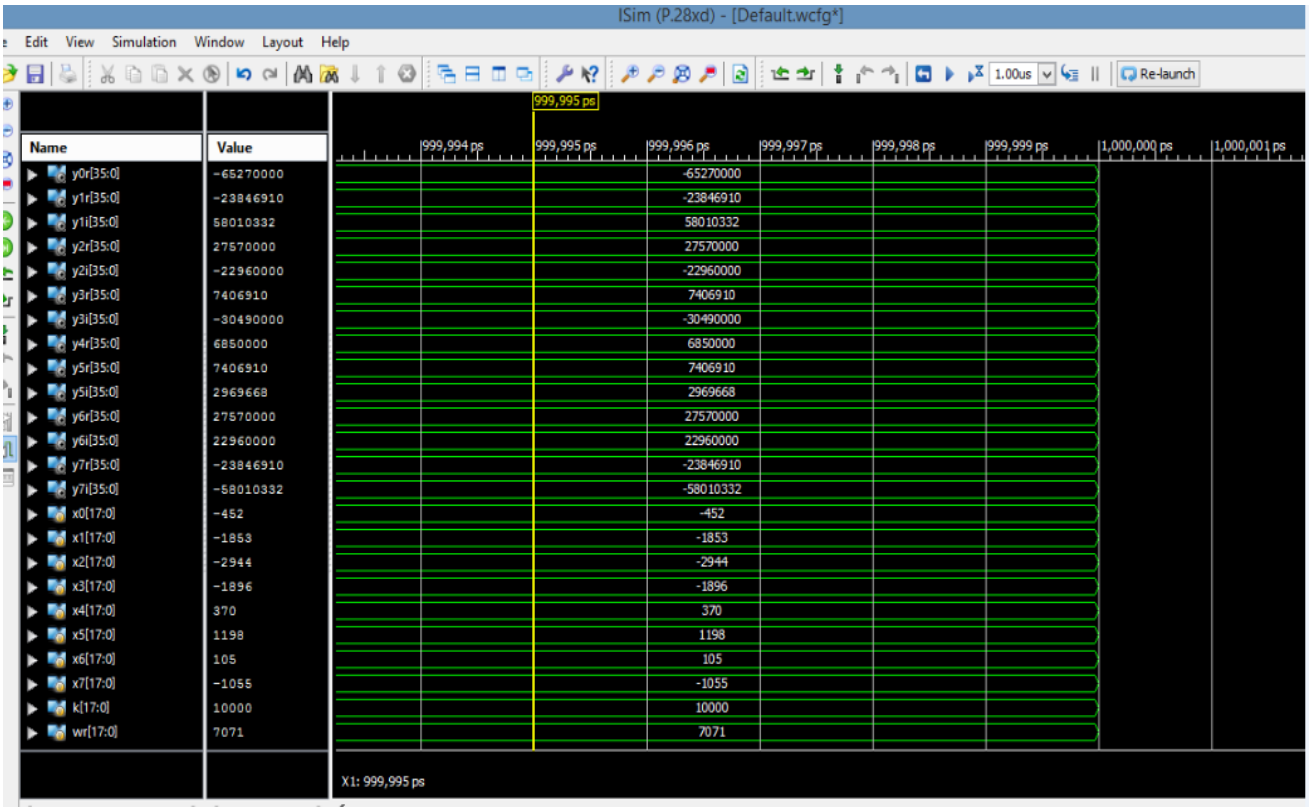

Fig. 5. Simulation Results of FFT with Booth-encoded Wallace Tree Multiplier shown in Signed Decimal Radix

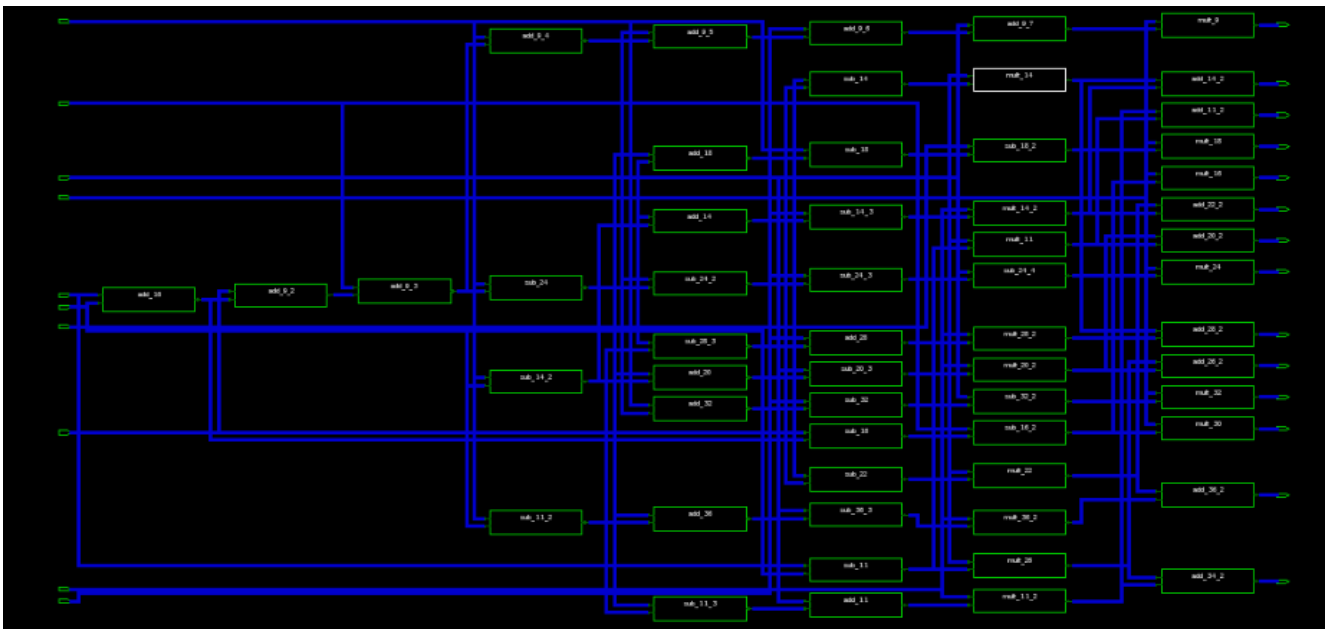

Fig. 6. Generic-Gate level Schematic of FFT with Booth-encoded Wallace Tree Multiplier

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V. FFT AND EEG

Virtually all sciences in the world contribute to the maintenance of human health and the practice of medicine. Medical physicists and biomedical engineers support the effective utilization of this medical science and technology as their responsibilities to enhance human health care with the new development of the medical tools such as Electroencephalogram. Electroencephalography (EEG) is a mechanism of measuring electrical activity of the brain. Upon studying EEG signals, various health conditions can be monitored and diagnosed e.g. Brain diseases like Alzheimer, Tumors, Head injuries, Epilepsy, Dementia, Human Behaviour, etc. These signals are recorded from various positions on scalp through electrodes and conductive media. Diagnostic results are made from the spectral content of EEG signals. Here comes the importance of FFTs in EEG signal analysis. They are extensively used in neuroscience, cognitive science and cognitive psychology due to its capability to reflect both normal and abnormal electrical activity of brain [1].

EEG signals are typically represented either through rhythmic activity or transients. Rhythmic Activity of brain signals is divided into different bands of frequency, namely, Delta, Theta, Alpha, Beta, Gamma. Table III. shows the frequency range of each band and the different states of the person [1]. Amongst these bands, Alpha band is widely used for various diagnostic studies [8]. Real-time applications like alerting drivers about their drowsiness through EEG variations in Alpha band is one of its kind. EEG signal analysis are crucial for evaluating Epilepsy. In marketing field, EEG signals have been used to study customer response to various products in market as a feedback method and product improvement study, referred to as neuro-marketing.

TABLE III. FREQUENCY BANDS IN EEG SIGNAL

EEG bands	Frequency band(in Hz)	Prominent
Delta	Less than 4	Deep sleep
Theta	4-7	Drowsiness
Alpha	8-13	Relaxed and awake
Beta	14-30	Sleep stages
Gamma	>30	Finger movements

In this work, EEG signal analysis is used to classify EEG levels of Autistic persons in Alpha band. Autism is a brain development disorder whose symptoms are visible since childhood. Autistic children due to seizures, show high delta and theta waveforms and low alpha waveform due to less metabolism. EEG signal pattern of normal persons are similar for similar age group, sex, race, food habits, environmental conditions, etc. However, frequency bands will remain the same for all people. Different types of special children show variations in EEG signals in Alpha band depending on their neurological function. Hence they can classified by comparing values of mid-frequency Alpha band of normal and Autistic persons.

EEG samples have been collected for a normal male aged at 21 years during closed eye condition based on 10 – 20 International Standards Electrode System with 19 channel electrode placement and 1 electrode as reference. FFT is computed for the two Occipital electrode position (O1 and O2) samples at a sampling frequency of 80 Hz in MATLAB. Power Spectral response is obtained to study and analyze Alpha band. Similarly, Radix-2 8-point DIT-FFT computation is performed using FFT implemented through Booth-encoded Wallace Tree Multiplier for the same sample.

Mid-frequency FFT value of Alpha band, at 10 Hz, are compared for the normal person. Values obtained through MATLAB and the FFT implemented circuit using Xilinx ISE is given in Table IV. Real-part values of the computed FFT at electrode O2 are plotted in Fig.7. Y-axis corresponds to real value of computed FFT and X-axis shows the corresponding frequency. Value at X0 = -0.0006527 volts is also shown in the figure.

TABLE IV. VALUES OF 8-POINT FFT FROM MATLAB AND XILINX ISE

Out-put	FFT using MATLAB (O2 electrode position) x 10^{-3} volts	FFT computed using VLSI circuit (O2 electrode position) x 10^{-11} volts
X0	-0.65257216 + j0.00000000	-65270000 +j0
X1	-0.23850908 + j0.58005815	-23846910 + j58010332
X2	+0.27570022 - j0.22963366	+27570000 - j22960000
X3	+0.07405211 - j0.02970924	+7406910 - j2969668
X4	11+0.06849303 + j0.00000000	+6850000+ j0
X5	+0.07405211 + j0.02970924	+7406910 + j2969668
X6	+0.27570022 + j0.22963366	+27570000 + j22960000
X7	111`-0.23850908 - j0.58005815	-23846910 – j58010332

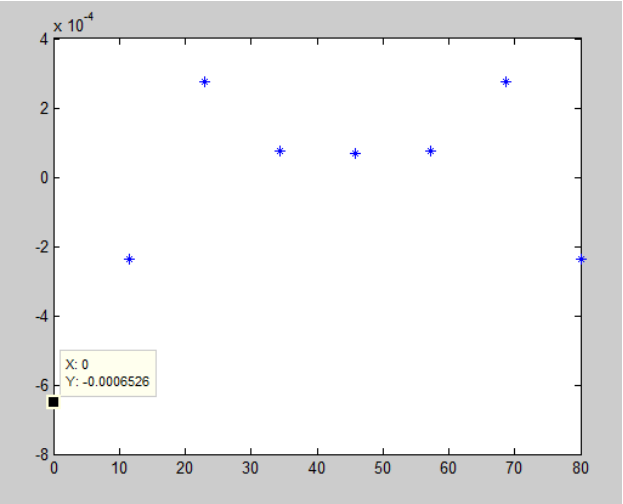

Fig. 7. Real-part values of the FFT output from MATLAB

VI. Results and Discussion

EEG data collected for a normal person has been sampled at 80 Hz in MATLAB. Delta band value X0 has been obtained as -0.0006526 volts. FFT has been implemented using Booth-encoder Wallace Tree multiplier to compute Radix-2 DIT-FFT algorithm. The same sample has been given as input to the FFT circuit in Test bench and delta band value is obtained as (-65270000 x $10^{-11)}$ volts. An accuracy of $\pm 0.019\%$ has been obtained through the implemented FFT circuit for all eight outputs obtained.

As per [1], Alpha band value of Autistic child is less than that of a normal child. The implemented FFT algorithm can be used to verify this result. Accuracy of computed Fast Fourier Transform value can be increased by increasing the significant digits of the twiddle factor ($1/\sqrt{2}$). The results obtained show an improvement in accuracy of +0.019% for four decimal places of twiddle factor ($1/\sqrt{2}$). Complexity of the circuit increases with increase in width of data.

VII. Conclusion and Future Scope

Generic-gate level implementation of Fast Fourier Transform using Booth-encoder Wallace Tree Multiplier has been done using VLSI 90nm technology. The circuit has been studied and analyzed for data accuracy and efficient performance. An accuracy of $\pm 0.019\%$ has been obtained for four decimal places of twiddle factor ($1/\sqrt{2}$). On increasing the number of significant digits of the twiddle factor, accuracy of output can be improved but it will share a trade-off with the area of the circuit. Physical level chip design and further optimization of the circuit in terms of area and power and increasing the number of points for FFT computation form the future scope of work.

Autistic EEG samples can be evaluated for the mid-frequency alpha band. This value is expected to be lower than normal person [1]. This circuit can thus be used to classify Autistic person based on EEG level and this work can be extended for its further analysis and verification.

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