

A 12bits 40MSPS SAR ADC with a redundancy algorithm and digital calibration for the ATLAS-LArg calorimeter readout

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Abstract—This paper presents a SAR ADC with a generalized redundant search algorithm offering the flexibility to relax the requirements on the DAC settling time and allowing a digital calibration, based on a code density analysis, to compensate the capacitors mismatching effects. The proposed architecture uses a DAC with only 2^{N-1} unit capacitors, for N-bit resolution, and a simplified monotonic switching algorithm. The design is fully differential featuring 12-bit 40MS/s in 130-nm 1P8M CMOS process.

Keywords—Digital calibration, Non-binary, Redundancy, SAR ADC, Switching algorithm.

I. INTRODUCTION

Particle detectors, such as liquid argon (LArg) calorimeter used in ATLAS experiment at the LHC (Large Hadron Collider), generate very large dynamic signals which require a sophisticated front-end electronics. This readout includes the noise optimization stages (low noise preamplifier, and analog multigrain filters), but one critical element is the Analog to Digital Converter (ADC). The requirements for our converter are 40MS/s at 12bits resolution. In this configuration pipeline architecture was widely used during this last years. But following the scaling of CMOS process, Successive Approximation Register (SAR) architecture appears to be more suitable in term of power dissipation. In this paper, a redundant SAR ADC is proposed, to achieve the high resolution required despite the capacitors mismatching. The paper is organized as follows. In Section II, the conventional SAR ADC is reviewed. Section III introduces the generalized non-binary search algorithm. Section IV presents the proposed redundant SAR ADC. In Section V, the design's simulations results are discussed.

II. CONVENTIONAL SAR ADC

Recently, SAR ADCs have been widely used for high-resolution, medium sampling rate, and low-power applications [1]. SAR ADCs are actually known to achieve very low power consumption owing to the extensive use of switching capacitor based circuits.

A SAR ADC is composed of a Sample and Hold S/H circuit, a comparator, a DAC, and a Successive Approximation Register logic circuit as shown in (Fig. 1): The analog input signal (V_{in}) is sampled by the S/H and compared with successive feedback voltage values (V_{DAC}) generated by the return DAC which is itself driven by a SAR algorithm designed

to minimize the error between V_{in} and V_{DAC} . N clock periods are required to resolve the N digital output bits. To execute this procedure, the conventional SAR ADCs uses a binary search algorithm following a binary-weighted capacitive DAC which is used also to perform the sample-and hold function [2].

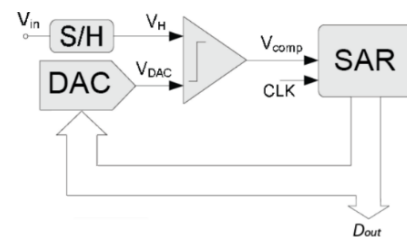


Fig. 1. Bloc diagram of a SAR ADC.

The drawback of the binary search algorithm is that it makes the ADC sensitive to decision errors due to capacitor matching limitations, incomplete DAC settling, parasitic capacitors, switch charge injections etc. Actually in case of an intermediate wrong decision, the following digitization process cannot recover, in Fig.2 the first comparison is wrong and this moves away V_{DAC} from V_{in} , which results in an error at the end of the conversion. Therefore one may guaranty an accuracy of quite 0.5LSB at each step of the SAR ADC processing. 12bits resolution for instance could not be achievable unless a big effort on matching is made for standard CMOS process.

We have created a Matlab model to evaluate just the capacitor matching limitations effects on a 12bits SAR-ADC. Simulation results are shown in Fig.3.



Fig. 2. Example of decision error due to incomplete DAC settling.

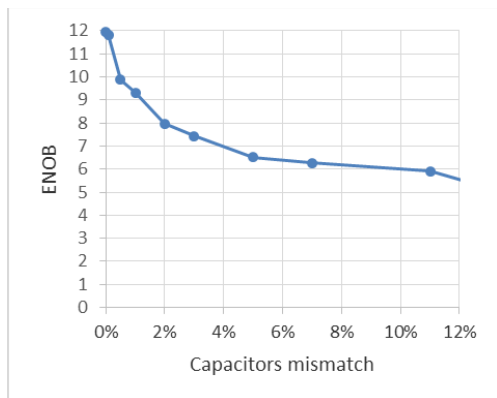


Fig. 3. Matlab simulations results for capacitors mismatch limitations on a 12 bits SAR ADC.

The pure binary search algorithm requires a strict and monotonic DAC section which is hard to combine with high density of integration that dramatically impacts the capacitor matching performances. To overcome these limitations, one solution is to move from the conventional binary search algorithm to a non-binary one.

III. GENERALIZED NON-BINARY SEARCH ALGORITHM

A non-binary search algorithm makes the SAR ADC tolerant towards incomplete DAC settling errors, and it makes possible a digital correction algorithm that corrects the capacitor mismatch errors, which is identified to be the main limiting factor for 12bits resolution ADCs and higher.

By using overlapped search ranges (redundancy), the non-binary search algorithm, compensates the comparison decision errors made in earlier conversion steps as long as the error made is within a certain tolerance range. To achieve an N-bit resolution using a redundant search algorithm, the SAR ADC requires M comparison steps ($M > N$) to determine the output digital bits, the idea is to have 2^M possible comparison combinations and 2^N possible digital output combinations, and since $M > N$, therefore $2^M > 2^N$. In other words, for a given output level D_{out} , there can be multiple comparison patterns leading to the same final result. Thus even if it happens for a comparison decision to be wrong, there is nevertheless a room for recovering a correct ADC output codes after the following steps. Fig. 4 illustrates an example of a 4-bit SAR ADC using 5-redundant steps.

Although, redundant search algorithm adds extra clock cycles to the conversion phase, the duration of these conversion steps can be made shorter (incomplete DAC settling) [4] and the overall conversion speed is then saved.

A SAR ADC implementing the non-binary search algorithm can use radix $r=2^{N/M}$ such as presented in [4] and [5]. An alternative method called "a generalized non-binary search algorithm" has been presented in [3] without restricting to radix of $2^{N/M}$. In each step (k) of conversion, to define the k -th bit, the analog input voltage is compared to a reference voltage ($V_{ref}(k)$) generated according to a redundancy vector p .

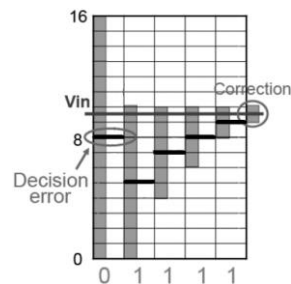


Fig. 4. Operation of a redundant search algorithm of a 4-bit 5-step SAR ADC.

Table-1 shows an example of the values of the redundancy vector p and the vector, of the acceptable errors, q in each step of conversion for a 12-bit 14-step SAR ADC.

TABLE I. A 12-BIT 14-STEP SAR ADC $p(k)$ AND $q(k)$ VALUES

Generalized non-binary search algorithm		
Step k	$p(k)$	$q(k)$
1	2048	24
2	1012	124
3	456	76
4	252	40
5	144	24
6	80	12
7	46	6
8	26	4
9	14	2
10	8	2
11	4	2
12	2	0
13	2	0
14	1	0

IV. PROPOSED ARCHITECTURE

To implement the generalized non-binary search algorithm for an N-bit conversion, based on a M-step redundant SAR ADC, a series of corresponding reference voltage must be generated and next been compared to the incoming voltage signal. In other words the ADC must perform the additions/subtractions, between $V_{ref}(k-1)$ and $p(k)$. For these operations a digital architecture approach is possible [3], but this strategy comes with an increase of the overall complexity of the design, and some extra delay and power consumption in the digital part of the ADC. Another approach is to perform the operations in the analog domain by using the DAC [6]. Each value of $p(k)$ is then stored in capacitor's values. This strategy presents the advantage of a reduced and simplified digital part of the circuit, which leads to reduced power consumption, compared to the one proposed in [3].

In this paper, we propose a fully differential N-bit M-step redundant architecture that implements the generalized non-binary search algorithm in the analog domain, a new structure is designed so as to only use 2^{N-1} unit capacitors in the DAC instead of 2^N in conventional solutions. This allows reducing the dynamic power consumption as well as the total capacitance

compared to the architecture proposed in [6]. Fig.5 shows the proposed architecture.

During the sampling phase, the differential input signal (V_{in+} and V_{in-} respectively) are stored on the capacitors array. After this phase, in each step, the ADC compares the input signal with the corresponding $V_{ref}(k)$ generated, by switching the corresponding capacitor, following the switching algorithm explained hereafter. The DAC is not segmented in order to perform a good linearity and avoid the limitations associated with split-capacitor structure such as the parasitic capacitance at the sub-DAC output and the fractional value of the bridge capacitor.

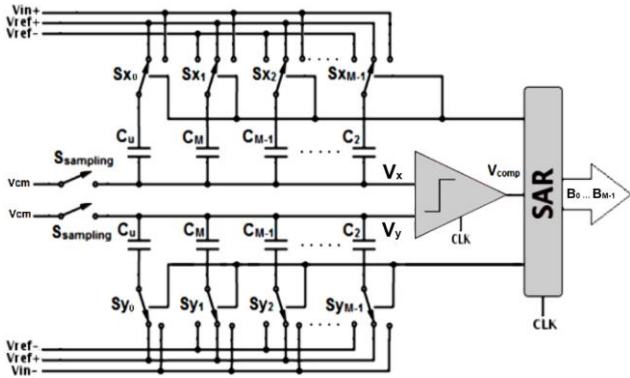


Fig. 5. The proposed N-bit M-step SAR ADC architecture (where $C_k=p(k)*C_u$ and $k = 2, 3 \dots M$).

The high speed low noise comparator is implemented by using a multi-stage differential pair as shown in Fig.6.

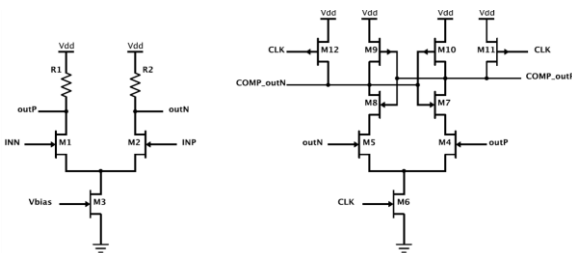


Fig. 6. Multistage comparator.

A. Proposed switching algorithm

The proposed redundant SAR ADC uses a simplified monotonic switching algorithm (see Fig. 7) which requires much less dynamic power consumption compared to the conventional switching algorithm.

One may notice that there is no switch-back operations and over the whole ADC, only one capacitor, is switched at each bit-cycle step, providing inherent immunity to the skew of the switch signals. At the end of the conversion, the N-bit digital output is calculated from the M-bit data. This proposed switching algorithm is also valid for the SAR ADC using the binary search algorithm, when $N=M$ and $C_k=2^{N-k}*C_u$; $2 \leq k \leq N$.

B. Digital Calibration

The digital calibration used with our ADC is based on [7], it uses the original ADC core without adding any extra analog hardware on-chip or any additional reference channel in the

design, and it is based on a statistical approach that uses a code density measurements to estimate the actual step sizes which map accurately the M-bit output into a final N-bit digitalized output.

In our case, a calibration signal is used to simplify the calibration algorithm presented in [7], during the calibration phase a full-scale ramp is sent to the ADC input to create a histogram of the 2^M possible output codes, after having normalized this histogram for the number of samples, an equation associated with each code bin is formulated, then an equations system is obtained by subtracting the neighboring equations. To calculate the estimated value of the step sizes the algorithm searches for a solution in this equations system.

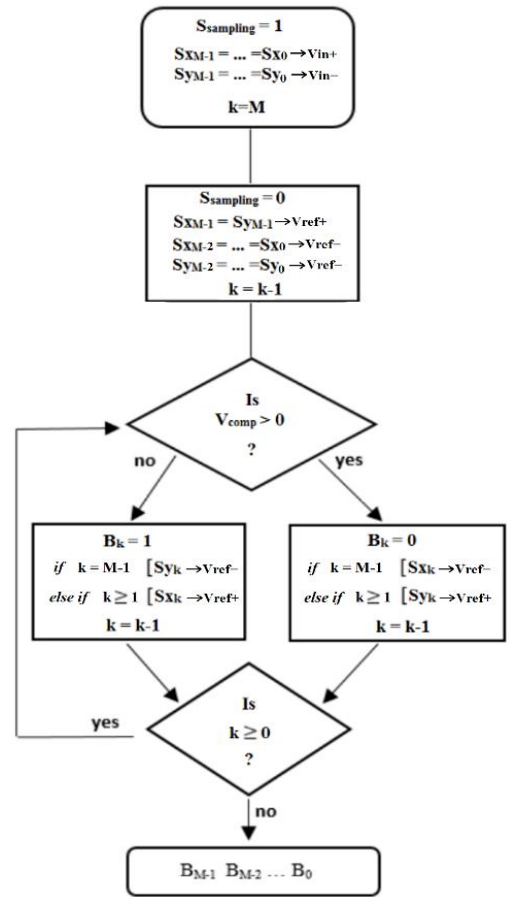


Fig. 7. Switching algorithm for the proposed SAR ADC.

V. SIMULATION RESULTS

Using the proposed architecture and the coefficients of Table.1, we designed in the 130-nm 1P8M IBM CMOS a fully differential 12bits redundant SAR ADC working at 40MSPS with a $2V_{pp}$ full-scale input range. Fig. 8 shows the layout of the redundant SAR-ADC designed and submitted to MOSIS run. The power consumption of the core ADC is about 25mW from a 1.5V supply.

Fig.9 shows the simulation results for the successive DAC approximation signal at the comparator input. In Fig.9 (a) all settlements are complete, therefore the ADC performs the conversion without any decision error, and the D_{out} calculated

from the 14bits is 3031. But in the configuration of Fig.9 (b) a wrong decision has been made in the second step due to an incomplete settling. However one can see how the ADC is capable to recover in the following steps, and D_{out} obtained finally is the same as in Fig.9 (a) (case without error). This illustrates the robustness of our redundancy architecture.

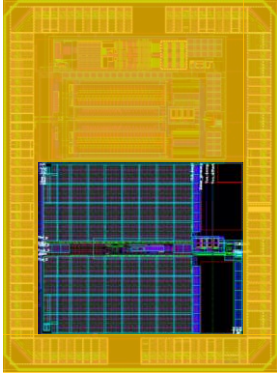


Fig. 8. The layout of the redundant SAR-ADC 12bit.

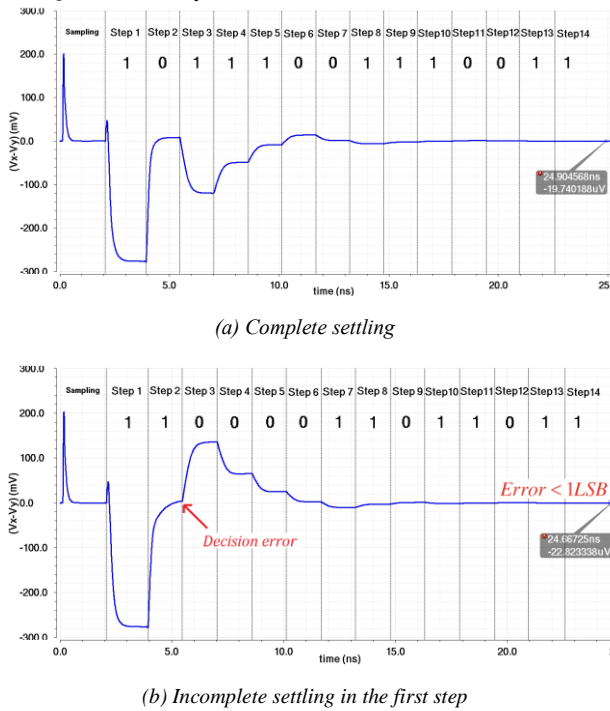


Fig. 9. The simulated DAC outputs voltage difference ($V_x - V_y$) of the proposed redundant architecture.

To evaluate the digital calibration regarding capacitor mismatching, a 5% capacitors mismatch error was inserted in the DAC and a 1.0546875MHz full-scale sine wave input was converted at 40-MSPS with 4096 samples, to simulate the static and dynamic performance. Fig. 10 and Fig. 11 show respectively the simulated INL and dynamic performance without and with calibration. Without calibration the maximum INL errors are $+56.5/-56.8$ LSB and the ADC achieves 38.25dB of SNR, 40.53dB of SFDR and 5.56b ENOB. After calibration the maximum INL errors is reduced to $+1.6/-1.7$ LSB and the ADC achieves 69.54dB of SNR, 64.23dB of SFDR and 11.15b ENOB.

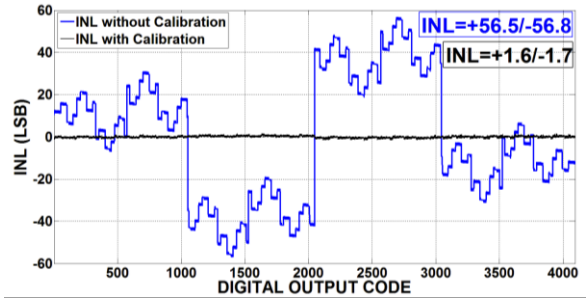


Fig. 10. The simulated INL without and with calibration.

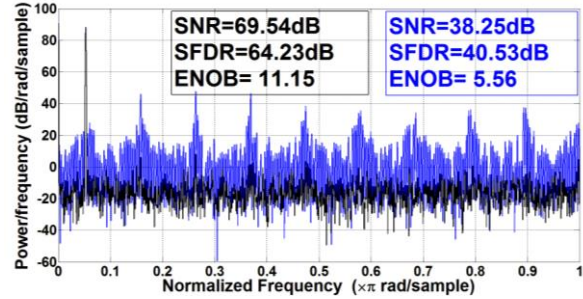


Fig. 11. The simulated FFT spectrum without and with calibration.

VI. Conclusion

A redundant SAR ADC has been presented with an efficient switching algorithm, and a digital calibration algorithm. The design of a generalized non-binary search algorithm is explained. Compared to previous works, this architecture presents the advantage of simplicity and minimizes the value of total capacitance. A design of a 12bits, 40MS/s configuration and its simulation results confirm the robustness of the proposed structure.

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