# A Novel Design of Low-power SRAM cell

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*Abstract*—SRAM cell is one of the most important part of FPGAs and Caches in digital design domain. This paper presents a new 8T SRAM cell with better performance (power consumption and delay time) than regular 6T and 8T SRAM cells. HSPICE simulations show that this new 8T SRAM cell has at least 43.7% improvement at power consumption in comparison with 6T SRAM cell based on 7nm technology model.

*Keywords—SRAM cell; power consumption; delay time; standby power; nanotechnology*

## I. INTRODUCTION

A digital system such as a computer is required memory to store data. Static Random Access Memories (SRAM) is usually made based on CMOS technology. In recent years the demand for low power devices has been increases tremendously. Also at the same time problems arising from continuous technology scaling have recently made power reduction an important design issue for the digital circuits and applications. SRAM based cache memories are best suited for system on chip applications due to its high speed and low power consumption.

One of the most effective approaches to meet this objective is to design SRAM cells whose operation is low power. However, with the aggressive scaling in technology, substantial problems have been encountered when the conventional six transistors (6T) SRAM cell configuration is utilized. In conventional SRAM cell because one of two bit-lines must be discharged to low (regardless of written value) the power consumption in both writing "0" and "1" are generally same [1]. Also during read operation, one of the two bit-lines must be discharged [3]. Therefore always there are transitions on bit lines in both writing "0" and reading "0". These cause high dynamic power consumption during read/write operation in conventional 6T SRAM cell. This cell shows poor stability at very small feature sizes and read static noise margins are small at 7nm. Therefore, an extensive literature can be found on designing SRAM cells for low power operation in the deep sub-micron/nano ranges [2] [4]. The common approach to meet the objective of low power design is to add more transistors to the original 6T cell. An 8T cell can be found in [2]; this cell employs two more transistors to access the read bit-line.

This paper proposed a new design for SRAM cell encountered in deep sub-micron CMOS ranges (7nm). This cell is that its design requires 8 transistors (8T). The process of the new 8T cell is compared with conventional 6T & 8T [2] cells. It is shown that this cell is better than 6T & 8T cells in terms of power consumption, stability, and access time. Simulation results using HSPICE confirm that the proposed new 8T cell is suited for implementation at 7nm CMOS technology, PTM models are used for HSPICE simulations.

## II. SRAM CELLS

### A. Conventional 6T SRAM cell

Current and read static noise margin (SNM) are two important parameters of SRAM cell. The conventional 6T SRAM cell has been found to be rather unstable at deep submicron/nano scale technology. The read SNM of cell shows the stability of cell during read operation and SRAM cell current determine the delay time of SRAM cell [5]. Fig. 1 shows the SRAM cell current in the conventional SRAM cell. Both Read SNM and SRAM cell current values are highly dependent on the driving capability of the access NMOS transistor. Read SNM decreases with increases in driving capability, while SRAM cell current increases [5]. That is, the dependence of the two is in an inverse correlation.

For solving the problem of inverse correlation between SRAM cell current and read SNM, a dual-port SRAM cell is composed of eight transistors, proposed in this cell data retention element and data output elements are separated each-others there for there will be no correlation between Read SNM and SRAM cell current.

### B. Existing 8T SRAM cell

To solve the decreased read SNM problem, the read and write processes are separated by adding read access structures to the conventional 6T cell. The read current does not affect the cell value, then the read stability of the 8T cell [2] is increased. Fig. 2 shows the scheme of an 8T SRAM cell. Write access to the cell occurs through the write access transistors (i.e. N1-N4, P1, P2) is identical to a conventional 6T SRAM cell and from the write bit-lines, BL and BLB. Read access to the cell is through the read access transistor N7, N8. This transistors are employed in to reduce the leakage current. Read operation controlled by the read word-line, RWL. Read bit-line, RBL is precharged prior to the read access. The word-line for read is also different from the write word-line.

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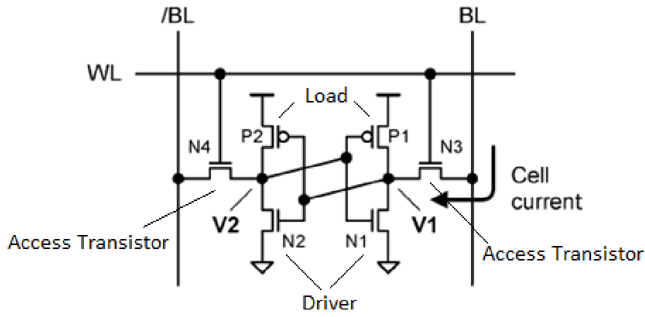


Fig. 1. Conventional SRAM cell

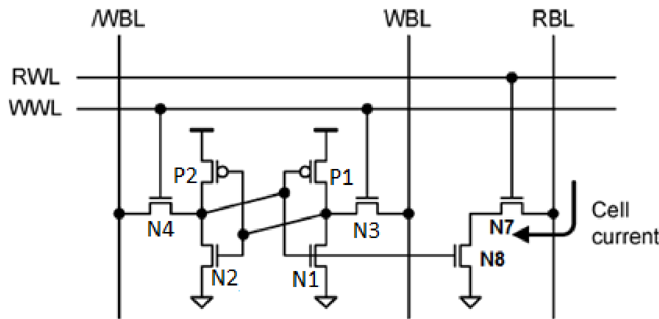


Fig. 2. Existing 8T SRAM cell

By doing this the worse-case stability position encountered previously in a 6T SRAM cell, is avoided and high read stability is retained prescribed; please do not alter them. You may note peculiarities. For example, the head margin in this template measures proportionately more than is customary. This measurement and others are deliberate, using specifications that anticipate your paper as one part of the entire proceedings, and not as an independent document.

### C. New 8T SRAM cell

Fig. 3 shows a nodified new 8T SRAM cell. Data protection NMOS transistor N5 for loop-cutting has been added between Node V2 and transistor N2. In our proposed new 8T-cell, $V_{th}$ in the NMOS N2 transistor are reduced, making it possible to achieve both low-$V_{dd}$ and high-speed operations. During write mode of cell While the SRAM cell is being accessed, /WWL is in the inactivated state, “0”, and N5 is OFF. Since N5 prevents the voltage at node V2 from decreasing, the data bit is not reversed even if node V1 voltage greatly exceeds. standby mode of cell read and write operation don’t perform on cell but signal /WWL is “1”, and transistor N5 is ON. The use of two CMOS inverters conclusions in high cell stability [Fig. 6, Fig. 7]. Figure 8 shows that the proposed new 8T cell has a higher
read SNM, comparing to the 8T SRAM cell.

One of the major advantages of this design is that it is necessary to prepare a precharge circuit as required in existing 8T SRAM cell and it is not necessary a sense amplifier circuit as required in 6T SRAM cell. Only when the RBL is changed, a charge/discharge power on the RBL is consumed.

## III. Read and Wright Operation

During write operation read-line (RWL) and /WWL maintained at GND. A write operation the memory cell will go through the following steps.

*1) Bit-line driving*: For a write, data drove on bit-line (WBL), and then word-line (WWL) asserted to VDD.

*2) Cell flipping*: this step includes two states as follows:

*a) Data is zero*: in this state, V2 node pulled down to GND by NMOS access transistor (N4), and therefore the Load transistor (P1) will be ON, and V1 node will be pulled up to VDD. Fig. 4 shows scheme of write "0" in the circuit.

*b) Data is one:* in this state, V2 node pulled up to VDD by NMOS access transistor (N4), and therefore the drive transistor (N1) will be ON, and V1 node will be pulled down to GND.

*3) Precharge mode:* The read bit-line, RBL , is precharged prior to the read access.

A read operation the memory cell is composed of two series transistors (N3 and N6) will go through the following steps. The word-line for read is also different from the write word-line. To start the read operation:

*1) RWL activation:* For a read, read bit-line precharged to vdd, and then floated. and read-word-line asserted to VDD during read operation.

*2) Write-word-line inactivation:* in this step write-word-line asserted to GND and two states can be considered:

*a) Voltage of V1 node is high:* when voltage of V1 node is high, RBL pulled down to GND through the transistor stack formed by N3 and N6. Fig. 5 shows scheme of read "0" in the circuit.

*b) Voltage of V1 node is low:* when voltage of V1 node is low, RBL remained to VDD becouse thetransistor N3 will be off.

*3) Standby mode:* At the end of read operation, cell will go to standby mode (when read and write operation don’t perform on cell) and read&write-word-line asserted to GND, respectively.

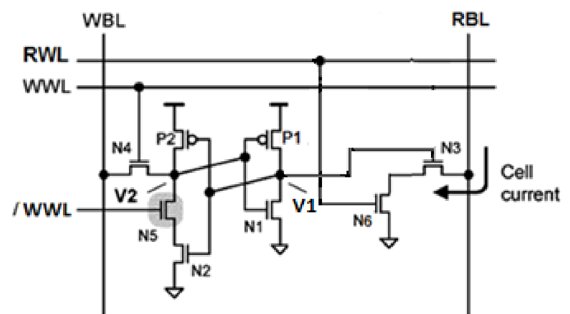


Fig. 3. New 8T SRAM cell

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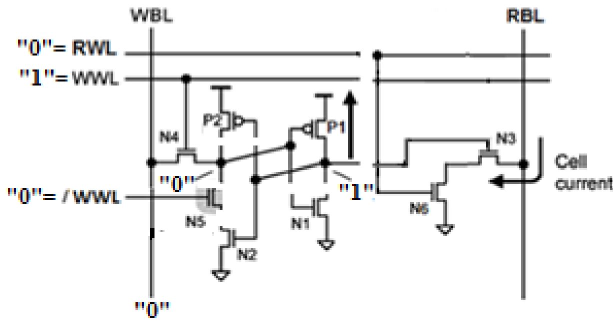


Fig. 4. Write "0" operation

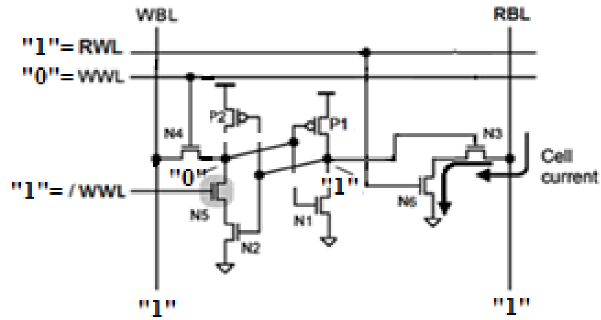


Fig. 5. Read "0" operation

## IV. Power Dissipation

Write power consumption of single ended structure is less because the bit line capacitance is reduced as compared to 6T double bit line switching.

$$Ps = \alpha ClVdd^2F_{cl} \quad (1)$$

Where Ps is switching power dissipation, α is activity factor, Cl is load capacitance and Vdd is power supply, $F_{cl}$ is input clock frequency [6].

As shown in Figure 9, the write power is significantly reduced with the proposed new 8T SRAM cell as compared to the conventional 6T SRAM cell. This reduction is due to the application of a single bit line for writing into the 8T SRAM cell in a memory column. For the 6T SRAM cell both bit lines in each memory column are periodically precharged to Vdd. When write operatione is constructed, one of the precharged bit lines is selectively discharged to Vss to do a write operation. Therefore, one of the bit lines needs to be fully charged and discharged during each write cycle, regardless of whether a 0 or a 1 is transferred to the cell. In case of writing a "1" to a memory column with the new 8T SRAM cell, the write bit line (WBL) does not need to be discharged. Then power consumption is significantly reduced. During read operation, the read power consumption is significantly reduced with the proposed new 8T SRAM cell as compared to the conventional 6T SRAM cell because the storage nodes (V2, V1) are completely isolated from the bit lines during a read operation.

## V. Simulation Results

In this section comparison between conventional 6TSRAM, new8T SRAM cell and 8T SRAM cell has been carried out on the basis read delay, average standby power and read & hold SNM (Table 1).

TABLE I. Comparison of average power dissipation during Standby operation , access time during read operation and read & hold SNM with the different combination of single VT and Low Vdd at 0.7v and 0.6v

| SRAM Cell | Supply Voltage(v) | Read SNM(v) | Hold SNM(v) | Av Standby Power(nw) | Read Access Time(ns) |
|---|---|---|---|---|---|
| 6T | 0.7 | 0.0711 | 0.125 | 297.33 | 1.4 |
| | 0.6 | 0.0915 | 0.050 | 230.97 | 1.35 |
| Existing 8T | 0.7 | 0.196 | 0.125 | 241.67 | 2.7 |
| | 0.6 | 0.119 | 0.0502 | 195.71 | 2.45 |
| New 8T | 0.7 | 0.203 | 0.217 | 229.83 | 2.75 |
| | 0.6 | 0.138 | 0.153 | 183.24 | 2.65 |

As you can see in Figure 8 by increasing the amount of voltage SNM increased and by reducing the amount of voltage SNM is reduced.

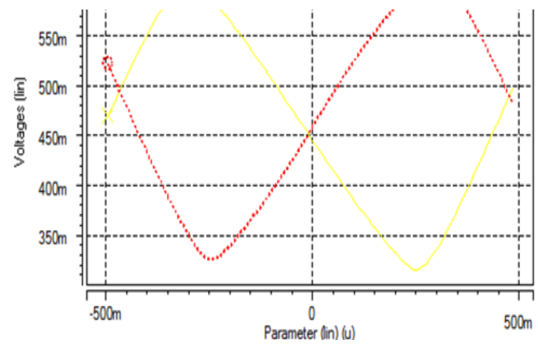


Fig. 6. Rotated (45°) Read SNM butterfly plot of a new 8T SRAM cell

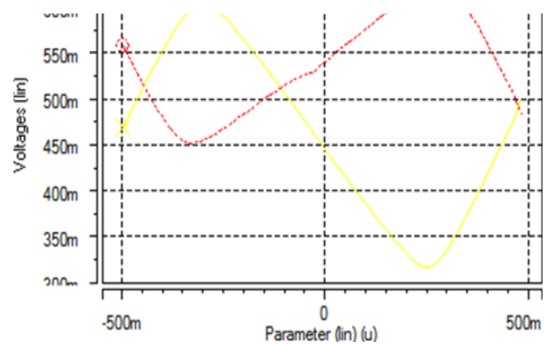


Fig. 7. Rotated (45°) Hold SNM butterfly plot of a new 8T SRAM cell

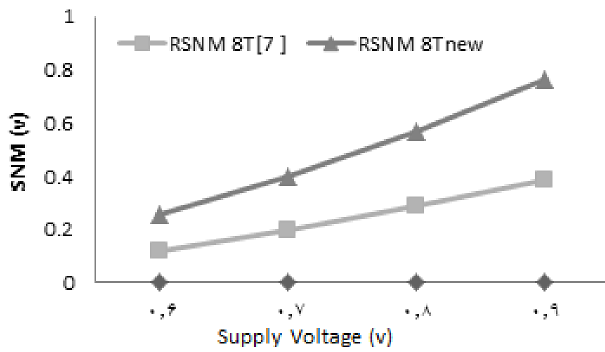


Fig. 8. Chart increase SNM by increasing the source voltage

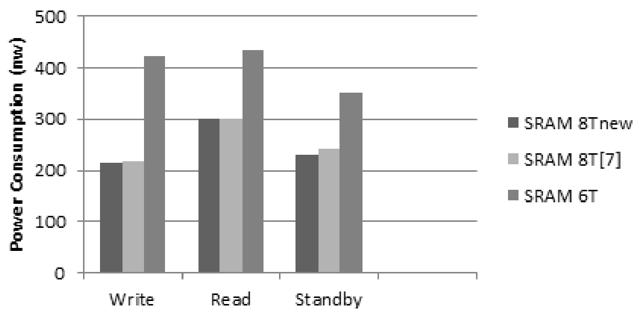


Fig. 9. Read,write and standby power consumption at 0.7V

## VI. CONCLUSION

The new 8T SRAM has been compared with respect to conventional 6T SRAM. Read delay of 8T SRAM cell is 20%, 0.5% better than 6T SRAM cell and 8T SRAM cell, because of the lower resistance of the read access delay path. Write delay of 8T SRAM is higher than conventional 6T SRAM and existing 8T SRAM cells due to utilization of only a single bit line for writing into the cells with the proposed technique.

New 8T SRAM when stored "0" and "1" respectively, has 49.16%, 54.02% less write power consumption as compared to 6T SRAM cell, and has 1.14%, 16.37% less than 8T SRAM cell [2]. This reduction in the write power is due to the utilization of a single bit line for writing into the new 8T and 8T SRAM [2] cells in a memory.

Read power consumption of new 8T SRAM when stored "0" and "1" respectively, is 30.53%, 43.72% better than 6T SRAM cell, and is 0.1%, 3.15% better than 8T SRAM cell due to advantage of low voltage of bit line during read operation.

In standby mode, power consumption of new 8T SRAM when stored "0" and "1" respectively, is 34.40%, 38.26% less than 6T SRAM cell, and is 4.89%, 5.53% less than 8T SRAM cell [2]. All the above simulations are done by 600mv as supply voltage and is shown a significant power reduction than regular cells.

The HSNM & RSNM & WSNM of new 8T respectively, is 42.39%, 3.44%, 12.14% high than 8T SRAM cell [2].

It is shown that this cell is better than 6T & 8T [2] cells in terms of power consumption, stability, and access time. Simulation results using HSPICE confirm that the proposed new 8T cell is suited for implementation at 7nm CMOS technology, PTM models are used for HSPICE simulations.

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