Effects of High-K Dielectric with Metal Gate for Electrical Characteristics of Nanostructured NMOS

Norani Bte Atan, Ibrahim Bin Ahmad, Burhanuddin Bin Yeop Majlis and Izzati Binti Ahmad Fauzi

***Abstract*—**This paper presents a systematic study of various high-K materials on metal gate MOSFET for 18nm NMOS. From this study, we find the suitable combination materials between the high-K and metal gate, and how it is a good affected on the electrical characteristics of 18nm NMOS. The device shows a good improvement on I_{on}/I_{off} ratio, where the higher ratio that means this device it is suitable for low power applications. The virtually designed and fabricated of the devices was performed by using Athena module. While electrical characteristic performance was stimulated by using Atlas module of SILVACO software. Physical models used for simulation from Al_2O_3, HFO_2, and TiO_2 as gate dielectric with TiSix as metal gate, which provide the higher physical thickness and reduce the leakage current. Excellent dielectric properties such as high-K constant, low leakage current, threshold voltage and electrical characteristics were demonstrated. From the simulation result, it was shown that HfO2 is the best dielectric material with metal gate, TiSix.

***Keywords*—**18 nm NMOS, High-K dielectric, Metal gate, Silvaco.

I. INTRODUCTION

New trend technologies, many industries have relied on a progression of smaller, denser, faster, cheaper and good quality of MOSFET. In order their main target is to reduce the production cost and at the same time can produce in big quantities of MOSFET. With increasing global competition, modern industries have to make their production process more efficient to compete. To do this, more advanced technologies have to be used. Scaling the MOSFET into nanometer regime, it is the best approach to solve many problems. It is a good and important challenging for future electronic technologies; refer to prospects of the scaling regime beyond 2011 ITRS [1].

Since MOSFET can be scaled down to smaller dimension which produce higher performance, at the same time gate length and oxide thickness also reduce. As the thickness scales of SiO_2 below 2nm, leakage currents due to tunneling increase drastically, leading to high power consumption and reduce device reliability. Therefore, replacing the SiO_2 with a high-K material allows increased gate capacitance [2]. The electrical characteristics of the device performance are analyzed with several of high-K materials and the gate oxide thickness is scaled to get same Equivalent Oxide Thickness (EOT). Recently, many researchers are focused on metal oxide materials with high-K values that have the ability to be integrated in MOSFET process flow. There are many high-K materials that are being studied nowadays such as Al_2O_3, HfO_2, and TiO_2 [3]. The best characteristics of gate dielectric should have high dielectric constant, large band gap with a favorable band alignment, low interface state density and good thermal stability. Among the high-K materials are compatible with silicon, and also materials have too low or high dielectric constant may not be adequate choice for alternative gate dielectric [4]. In this paper, we compare the electrical characteristics results for Titanium Silicide (TiSix) fabricated on Al_2O_3 (k~9), HfO_2 (k~25) and TiO_2 (k~85) gate dielectric. Thus the performance for all high-K materials with TiSix are explored and presented in the following section.

II. MATERIALS AND METHODS

This paper is presenting the fabrication of 18nm NMOS. The specification of the sample used in this experiment was p-type (boron doped) silicon substrate with doping concentration of $7x10^{14}$ atoms cm^{-3} and <100> orientation. The next procedure is to develop the P-well with growing a 200 Å oxide screen on the top of bulk silicon. This method using dry oxygen at high temperature 970°C followed by Boron as dopant with a dose of $3.75x10^{13}$ atoms/cm^3. The oxide layer as a mask was etched after the completed process of P-well doping. The next step was annealing process to ensure all boron atoms being spread uniformly in the wafer at 900°C with nitrogen and followed by 950°C with dry oxigen. The next step was preparing the isolate neighboring transistor or Shallow Trench Isolator (STR) of 130 Å thicknesses [5]. After that, the wafer was oxidized with dry oxygen for 25 minutes at 900°C. There were two important process involved in developing of STI such as Low Pressure Chemical Deposition (LPCVD) and Reactive Ion Etching (RIE). LPCVD process was applying with 1000 Å nitride layer was deposited on top of the STI oxide layer, followed by a photo resistor was deposition on the wafer. Then, RIE process was etching the unnecessary part on the top of STI area. Chemical Mechanical Polishing (CMP) was implementing to etched extra oxide on the wafer. STI was annealed for 15 min at 900°C. A sacrificial oxide layer was developed and etched to eliminate defects on the surface [6]. The process of STI was completed.

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Between the channel regions, the deposition of high-K materials (Al_2O_3, HfO_2, and TiO_2) process with gate oxide thickness is scaled so that they have the same EOT with SiO_2 by analyzed electrical characteristics of the device. The length of the high-K material was scaled to get 18nm same as the gate length of transistor. Then, the implantation dose of boron on the N-well active area for the threshold voltage (V_{th}) adjustment process. Next, the Titanium Silicide (TiSix) deposited on the top of high-K materials (Al_2O_3, HfO_2, and TiO_2) and followed by halo implantation with adjusted of indium dose to obtain the optimum value of the NMOS device [7,8]. The next process was formation of the sidewall spacer. It used as a mask for source and drain implantation. In this case, implantation with arsenic dose and followed by phosphor dose respectively. It was to ensure the smooth current flow in NMOS device [9].

The next step was development 0.5 μm layer of Boron Phosphor Silicate Glass (BPSG). This layer acted as the Pre Metal Dielectric (PMD) [10]. Again, annealing process was done on the wafer to strengthen the structure under temperature 950°C. The last process of wafer was compensation implantation which using the phosphor dose. From the above experiment, the dosages quantities for boron, indium, arsenic, and phosphor were different which based on the high-K materials (HfO_2, TiO_2 and Al_2O_3). The last step was deposition of aluminum layer as the metal contact for source and drain. Therefore, under ATHENA module the design of 18nm NMOS structure already completed. There are many factors influence as the input process parameters on the threshold voltage 18nm NMOS such as Gate oxide thickness, Substrate implant dose, Pocket-halo implant tilt angle, Gate oxide diffusion temperature, V_{th} implant dose, V_{th} implant energy, Pocket-halo implant energy, Pocket-halo implant dose, S/D implant dose, S/D implant energy, Compensation implant dose and Compensation implant energy. Now, we will proceed the stimulation process under ATLAS module to measure the electrical characteristic such as I_D versus V_{DS}, I_D versus V_{GS}, I_{on}, I_{off}, and V_{th}.

III. RESULTS AND DISCUSSIONS

The complete fabrication of 18nm NMOS has been modeled and simulated successfully in Silvaco Simulink. Figure 1 shows the complete 18nm gate length NMOS. Figure 2 shows clearly on the doping profile of one of the design structure with gate length 18nm NMOS.

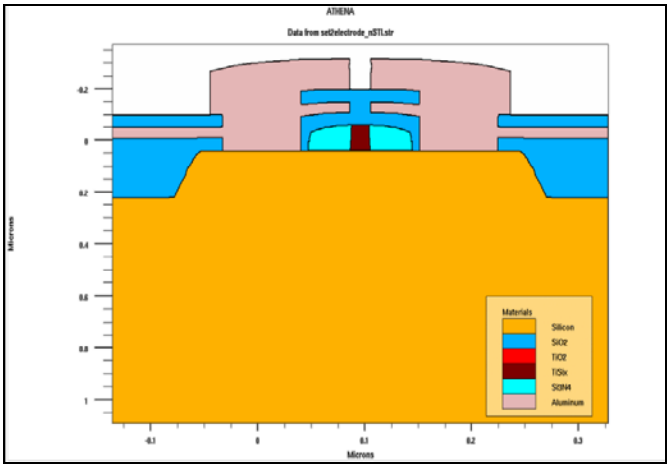

Figure 1. NMOS cross section after Fabrication Simulation

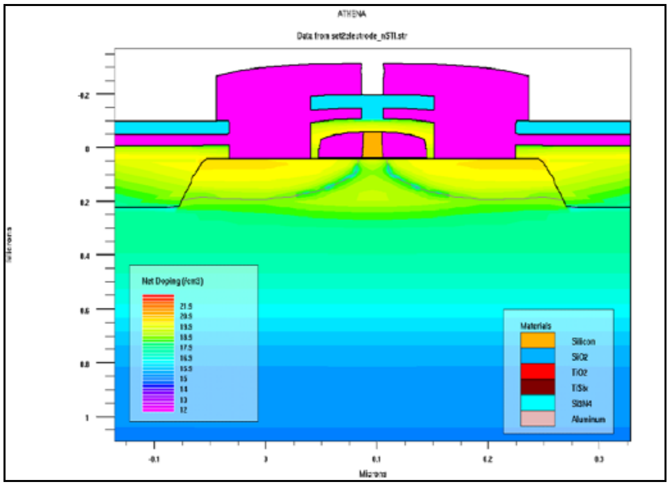

Figure 2. Doping profile of 18nm gate length NMOS with TiO2 dielectric and TiSix metal gate

Results of electrical characteristic simulation are obtained in Figure 3 for I_D –V_{DS} and Figure 4 for I_D – V_{GS} with different materials of high-K such as Al_2O_3 (k~9), HfO_2 (k~25) and TiO_2 (k~85). Voltage, $V_{GS} = 2.6$ volts is applied for I_D –V_{DS} graph with different voltage of V_{DS}. While, $V_{DS} = 1.4$ volts is supplied for I_D – V_{GS} graph with different V_{GS} voltage. The threshold voltage (V_{TH}), state on current (I_{on}) and state off current (I_{off}) can be extracted from I_D –V_{GS} curve.

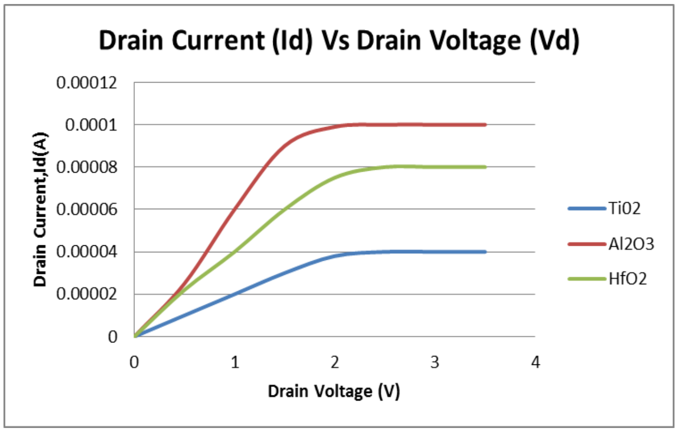

Figure 3. I_D Versus V_{DS} characteristic for different of high-K dielectric constants (k)

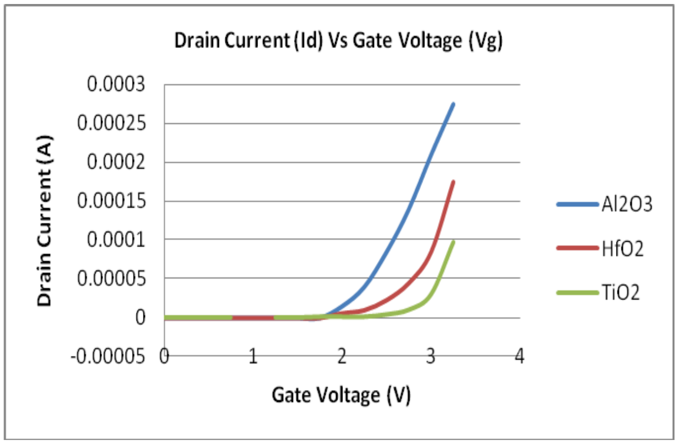

Figure 4. I_D Versus V_{GS} characteristic for different of high-K dielectric constants (k)

A good doping concentration is one of factor to ensure the transistor works well with fewer leakage current and enhance gate control [11]. There are four factors that influence in the threshold voltage counter measure such as Threshold voltage ajustment implant, Halo implant, Channel implant and Compensation implant. But for this research, only changing the various of dielectric material (Al_2O_3, HfO_2 and TiO_2) on the TiSix of transistor, so the Threshold voltage ajustment implant is best doping concentration to get a threshold voltage (V_{TH}) 0.302651 with 6.03036 x 10^{13} cm^{-2} boron for Al_2O_3. To maintain the same value of V_{TH}, due to the physically thicker dielectric layer, therefore the boron doping for HfO_2 and TiO2 were increased to 8.53256 x 10^{13} cm^{-2} and 9.73654 x 10^{13} cm^{-2} respectively. The increase of V_{TH} adjustment implant doping concentration was proportional with increasing the value of high-K dielectric, and at the same time the values of drain current (Ion) were decreased as shown in Figure 5.

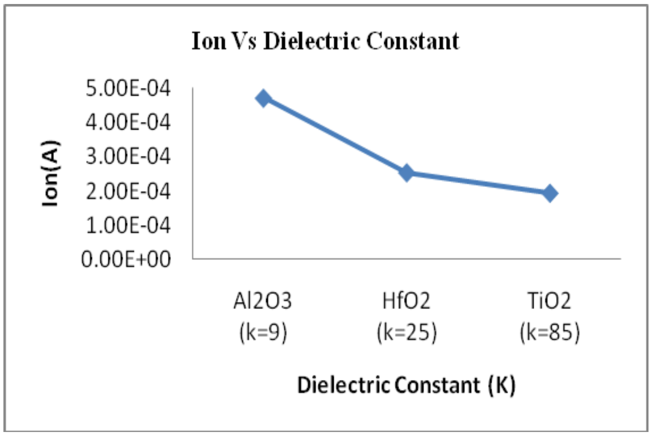

Figure 5. I_{on} current for Al_2O_3, HfO_2 and TiO_2 dielectric

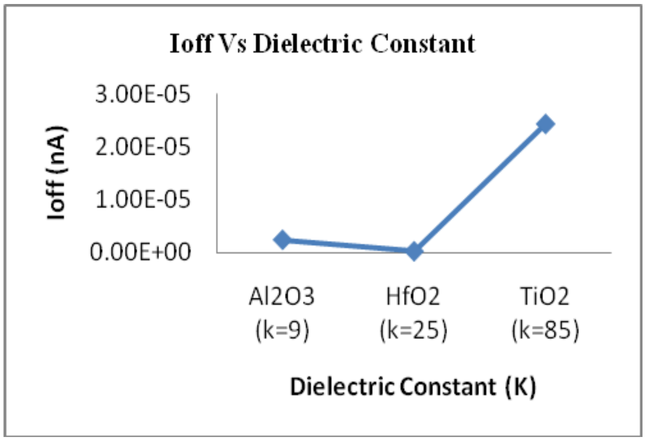

Figure 6. I_{off} current for Al_2O_3, HfO_2 and TiO_2 dielectric

Drain leakage current (I_{off}) or sub-threshold leakage current occurs when the gate voltage (V_{GS}) is lower than the threshold voltage (V_{TH}). In ideal case, when the transistor is turned off, V_{GS} = 0 volt and V_{DS} = V_{DD} (voltage supply), there is no current can through into the channel (I_{off} = 0). Refer to Figure 6, the leakage current for HfO_2 dielectric is lowest compared with Al_2O_3 and TiO_2 dielectrics. It is means, HfO_2 dielectric material most compatible with silicon and most stable oxide with the highest heat of formation [12,13].

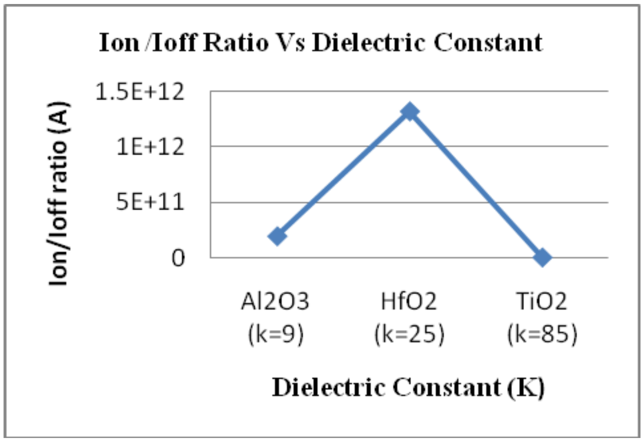

Figure 7. I_{on}/I_{off} current for Al_2O_3, HfO_2 and TiO_2 dielectric

Figure 7 shows the I_{on}/I_{off} current for different materials of high-K dielectric. HfO_2 dielectric gives the highest I_{on}/I_{off} ratio compared with Al_2O_3 and TiO_2 dielectrics. Hence, better performance of device can be obtained by using HfO_2 dielectric as gate oxide. This device is suitable for low power application [14].

Table 1. Simulated Results of Various Dielectric materials With ITRS 2011 Prediction

Parameter	**Simulation**			**ITRS 2011 Prediction**
	Al_2O_3	HfO_2	TiO_2	
V_{TH} (V)	0.302651	0.302651	0.302651	0.302
I_{on}	$4.7212\mathrm{x}10^{-4}$	$2.5355\mathrm{x}10^{-4}$	$1.9336\mathrm{x}10^{-4}$	$1.0\ \mathrm{x}\ 10^{-7}$
I_{off}	$2.3652\mathrm{x}10^{-15}$	$1.9123\mathrm{x}10^{-16}$	$2.4316\mathrm{x}10^{-14}$	$1.496\ \mathrm{x}10^{-6}$
$I_{on}/\ I_{off\ ratio}$	$1.9961\mathrm{x}10^{11}$	$1.3259\mathrm{x}10^{12}$	$7.9519\mathrm{x}10^{9}$	$6.6845\mathrm{x}10^{-2}$

Table 1 shows the simulated results for Al_2O_3, HfO_2 and TiO_2 dielectric materials with TiSix as metal gate for 18nm NMOS. I_{on} results from the simulation are bigger value compared prediction value. While the simulation results for I_{off} are lower than prediction value. Therefore, all the above high-K materials are suitable with metal gate and compatible with silicon of transistor. But the best choice is HfO_2 as dielectric of transistor.

IV. CONCLUSION

NMOS structure with 18nm were successfully designed and stimulated to study the various of dielectric materials on metal gate of device performance. The performance of the three dielectric materials, Al_2O_3, HfO_2 and TiO_2 with TiSix as metal gate were compared and it was found HfO_2 is the best dielectric material for the future nano scale MOS devices technology. It based on the highest value of I_{on}/I_{off} ratio, and lowest value of sub-threshold leakage current (I_{off}). It is suitable for low power application.

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