A 5-tap Half-rate DFE Receiver for Data-Edge Simultaneous Equalization

Sung-Won Choi, Hyun-Wook Lim, and Bai-Sun Kong

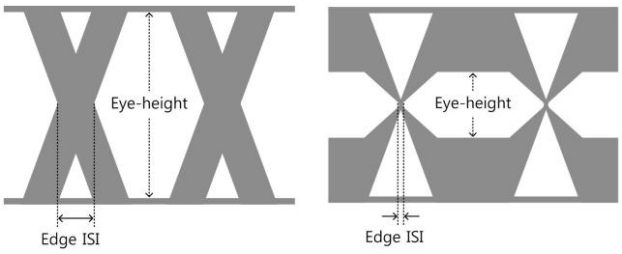
***Abstract*—**The paper presents a 5-tap half-rate DFE receiver for data-edge simultaneous equalization. The proposed DFE receiver can cancel ISIs at data transition edges as well as at data sampling points by employing a novel equalization method based on received waveform shaping. The proposed DFE receiver is designed in a 45-nm LP CMOS process. The evaluation results indicate that edge ISI is reduced by 30% with no degradation on data ISI cancellation. It also indicates that the output jitter of a CDR designed with the proposed DFE is reduced by 19% compared to the conventional data-based DFE.

***Keywords*—**Decision feedback equalizer, data-based DFE, edge-based DFE

I. Introduction

As the data rate of an electric channel increases, inter-symbol interference (ISI) is getting larger due to limited bandwidth of the channel. The decision feedback equalization (DFE) is commonly used to solve this problem [1]. A traditional DFE approach that is called the data-based DFE (D-DFE) [2], [3] cancels post-cursor ISIs without amplifying noise. Fig. 1(a) shows the eye diagram of a D-DFE, in which we can recognize that the voltage margin at the center of a data eye is extended. But, unfortunately, the timing margin at data transition edges is still not enough due to a large amount of edge ISI.

CDR used for clock and data recovery usually takes advantage of timing information derived from zero-crossing points or transition edges of received signals. To get the timing information, CDR often uses an edge sampler that samples signal values at transition edges. Thus, if the equalized signal has a large amount of ISI at transition edges, the recovered clock may not have transitions at required timing points, resulting in an unreliable sampling of the channel data. Hence, minimizing the edge ISI at CDR input is very important for reducing the deterministic jitter at CDR output [4] and for improving the jitter tolerance of a CDR. Recently, edge-based DFEs (E-DFEs) [5], [6] are proposed to minimize the amount of ISI at data edges. The eye diagram of an E-DFE is depicted in Fig. 1(b), which indicates that the E-DFE have reduced the edge ISI substantially. But, as can be seen by the figure, there is an incomplete mitigation of ISI at data centers, resulting in an eye height reduction. A recent DFE receiver [7], [8] tries to reduce timing jitter without the degradation of eye height. The receiver uses a D-DFE for input data equalization and an E-DFE for edge data equalization. But, in this implementation, separate D-DFE and E-DFE with the same architecture have been employed. So, the approach is considered to be a bulky and power-hungry solution due to doubled area and power dissipation.



(a) (b)

Fig. 1. Eye diagram of (a) data-based DFE and (b) edge-based DFE

This paper introduces a novel DFE architecture to eliminate ISIs at data edges and centers simultaneously using a single equalizer. The proposed DFE equalizes the entire shape of the response to eliminate both the edge and data ISIs simultaneously. The remaining sections are as follows. Section II describes the proposed DFE concept and implementation details of a 5-tap half-rate DFE receiver embedding the proposed scheme. The performance comparison is presented in Section III. Section IV concludes the paper.

II. Proposed 5-tap Half-rate DFE

A. Equalization Concept

The conceptual comparison between the conventional D-DFE and the proposed waveform-shaping DFE (WS-DFE) to equalize received signal are represented in Fig. 2. Limited bandwidth of the channel attenuates received signal for a single-bit pulse (Fig. 2(a) and (d)). The shaded region in these figures represents the area eliminated by each DFE. As for the

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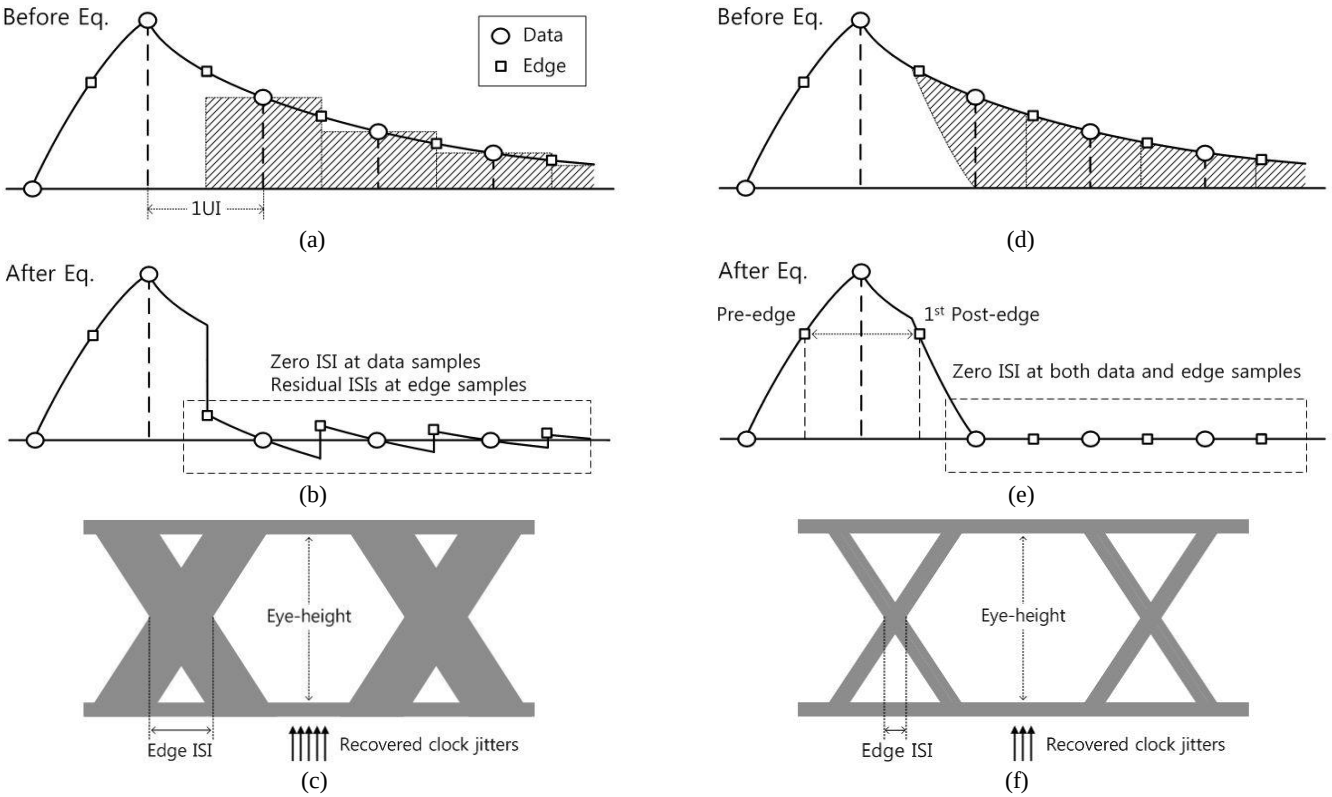


Fig. 2. Single-bit pulse response (a) before equalization, (b) after equalization, and (c) eye diagram for conventional data-only DFE. Single-bit pulse response (d) before equalization, (e) after equalization, and (f) eye diagram for proposed waveform-shaping DFE.

conventional approach, tap coefficients for equalization are basically constant, and set only to eliminate ISIs at data centers. So, they are not able to thoroughly eliminate ISIs at transition edges (Fig. 2(b)). The resulting residual ISIs at edge samples reduce the horizontal eye opening of received data (Fig. 2(c)), and make more jitter of recovered clock as explained previously. Reduced horizontal eye opening and larger clock jitter cannot ensure a reliable operation of the receiver.

Meanwhile, as for the proposed approach, tap coefficient values do not remain constant, but are made to be variable and adjusted to properly tailor or cancel the whole shape of ISIs in a single-bit pulse response. More specifically, for providing accurate timing information to CDR and stable data information to slicers, the magnitude of ISI at the first post-edge point is set equal to that at the pre-edge point [6], and the remaining ISIs at following data and edge sampling points are all eliminated (Fig. 2(e)). The resulting substantial reduction of edge ISIs extends the horizontal eye opening (Fig. 2(f)), and allows jitter reduction of recovered clock. Wider horizontal eye opening and reduced jitter will foster a reliable operation of the receiver.

Detailed diagrams to show how the proposed WS-DFE can reshape the single-bit pulse response in Fig. 2(d) into the desired form in Fig. 2(e) are illustrated in Fig. 3. Fig. 3(a) highlights by slash lines the area to be cancelled by the first tap. To eliminate this area, the proposed DFE tailors three ISI sub-areas (area A, B, and C), as shown in Fig. 3(b)-(e). Areas A and B are first subtracted from the received waveform (Fig. 3(b)), resulting in a tailored waveform (Fig. 3(c)) where zero ISI at the first post-edge and post-data cursors. A DFE tap with a constant current can be used to cover area A, and another DFE tap with a variable current can cover area B. At the same time, area C is added to match the magnitude of the first post-edge with that of the pre-edge, resulting in the waveform shown in Fig. 3(d). A DFE tap with another variable current can cover area C. Then,

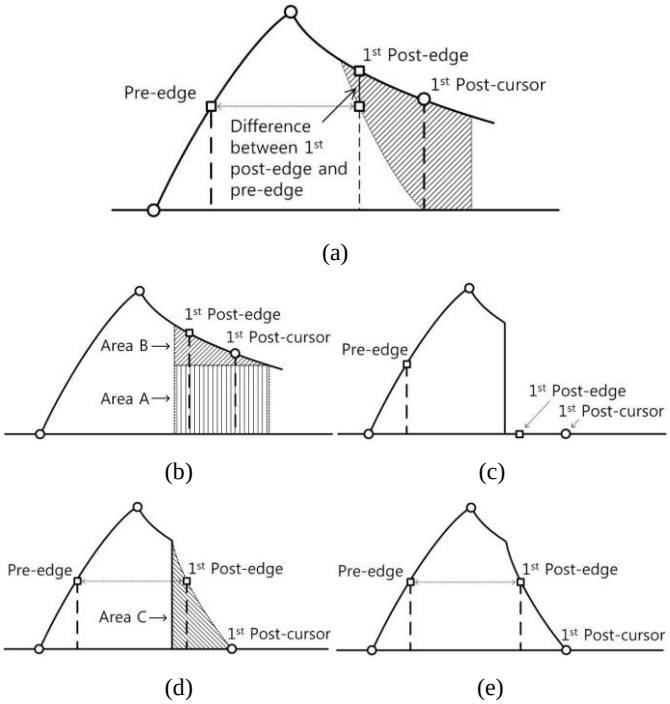


Fig. 3. Waveform reshaping for eliminating edge and data ISIs.

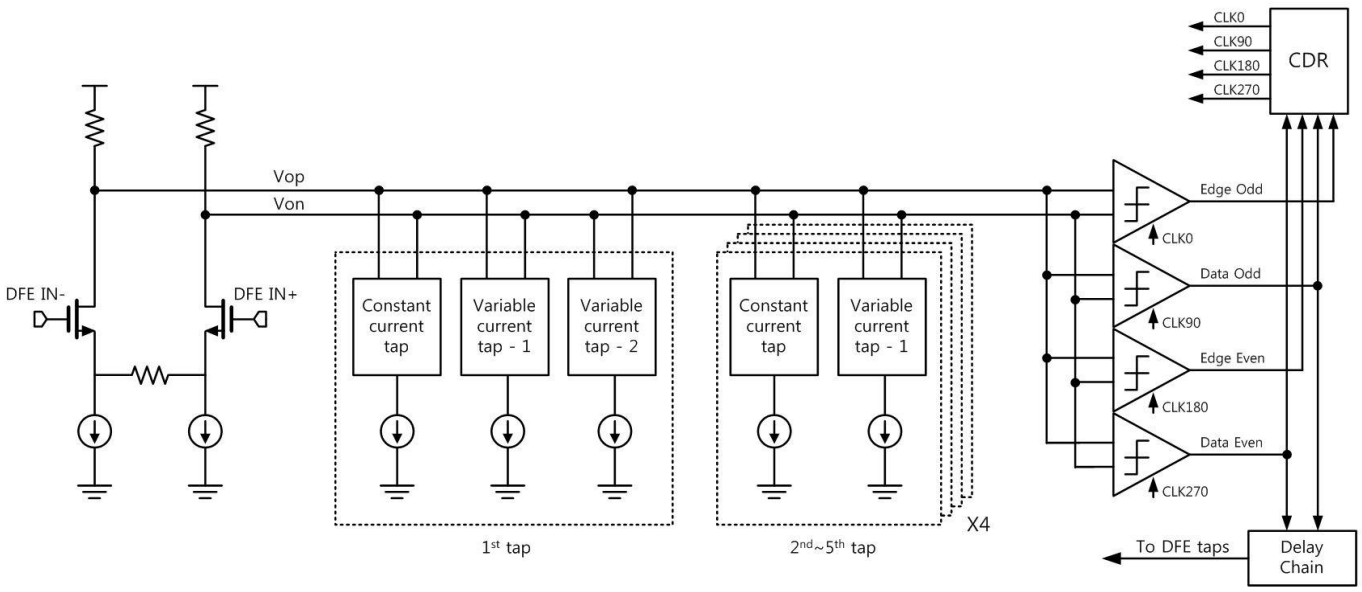


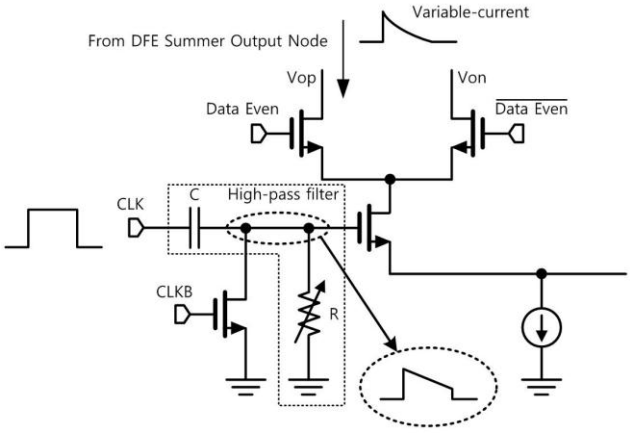
Fig. 4. Overall architecture of proposed WS-DFE

as shown in Fig. 3(e), the first post-edge and the pre-edge will have the same magnitude, and ISI at the first post-cursor point will be zero. For the other taps, a tap with a constant current and another tap with a variable current are used to eliminate ISIs at edge and data sampling points like Fig. 3(b) and (c).

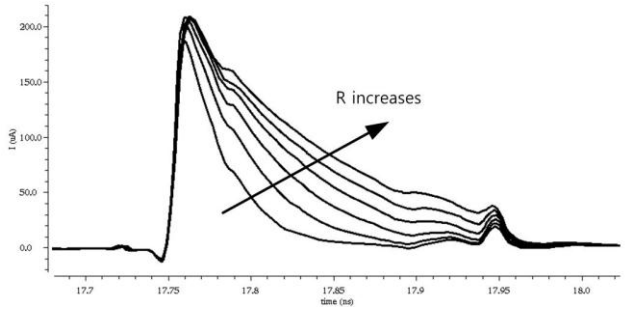
B. Equalizer Implementation

The overall architecture of the proposed 5-tap half-rate WS-DFE is depicted in Fig. 4. It adopts the current-summing amplifier with resistive load, and is operated by half-rate differential clock. The summing nodes of the DFE are driven to slicers for data sampling, and the sampled data are fed into CDR for clock and data recovery. In the proposed DFE, as mentioned earlier, one constant-current tap and two variable-current taps are used for the first tap, whereas one constant-current tap and one variable-current tap are used for all the other taps in the receiver.

The structure of the constant-current tap in the proposed WS-DFE is the same as that of the tap in the conventional D-DFE. The structure of the variable current generator for the variable-current tap is shown in Fig. 5(a). The opposite side of the generator is complementary to the circuit shown here. A high-pass filter is used for generating the required variable current. After the clock passes through the RC high-pass filter, the pulse described in Fig. 5(a) is generated at the high-pass filter output, which turns the switch transistor on and turns it off gradually. To adjust the shape and magnitude of the tap coefficient, the value of R and the current of I-DAC are tuned. The shape of the current is controlled by changing the value of R. The peak value of the current is determined by the amount of the I-DAC current. Adjustment of the variable current according to the change of R is shown in Fig. 5(b). As the resistor value increases, the slope of the current becomes gradual. A proper value of R can be used to adjust tap coefficient values to cancel the overall shape of the ISI for a single-bit pulse response.



(a)

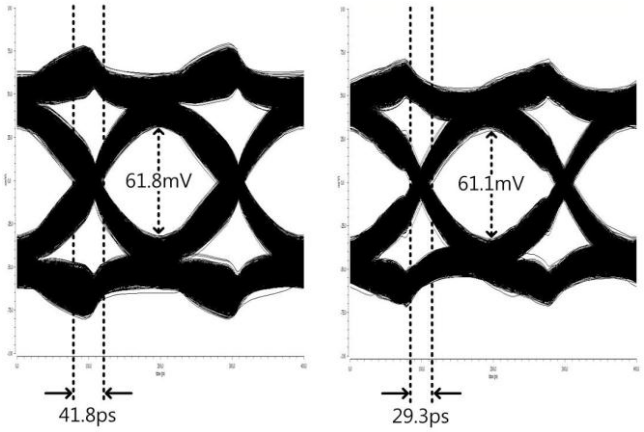


(b)

Fig. 5. Variable current generation: (a) circuit diagram, (b) current vs. resistance

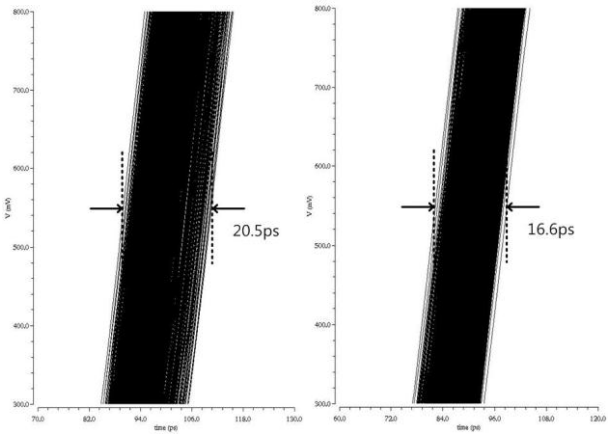
III. Simulation Results

The proposed 5-tap half-rate DFE receiver was designed in a 45-nm LP CMOS process. A 40" FR4 trace with 16dB loss at 2.5GHz including receiver package loss was used as the channel. Transmit swing is set to 200mVpp. The proposed DFE receiver



(a) (b)

Fig. 6. Simulated eye diagram; (a) conventional D-DFE, (b) proposed WS-DFE



(a) (b)

Fig. 7. CDR output jitter with (a) conventional D-DFE and (b) proposed WS-DFE

is clocked by 2.5GHz differential clock to operate at 5Gb/s or 200ps UI at 1.1 V. Fig. 6 shows simulated eye-diagram for the conventional D-DFE and proposed WS-DFE receivers. As shown by the figure, the proposed DFE has a reduced ISI at edges without degrading the eye height. The amount of edge ISI of the conventional DFE is 41.8ps, whereas that of the proposed DFE is 29.3ps, indicating 30% improvement.

The reduction of edge ISI of the proposed WS-DFE will lead to an improvement on jitter performance of CDR. To verify this aspect, a CDR with bang-bang phase detector (BBPD) [9] is implemented. The CDR uses a half-rate phase-locked loop (PLL) for clock recovery, consisting of BBPD, loop filter, VCO and clock buffers. The comparison between the jitter performance of CDRs with the conventional D-DFE and with proposed WS-DFE is shown in Fig. 7. It indicates that the jitter of the CDR with the proposed DFE is reduced from 20.5ps to 16.6ps, resulting in 19% improvement. Table I summarizes the performance of DFEs, such as the number of taps, vertical and horizontal eye-opening, edge ISI, and CDR jitter. The conventional D-DFE and proposed WS-DFE use the same number of taps to allow the same capacity to cancel ISIs at data sampling points. The proposed WS-DFE reduces edge ISI by 30% resulting in 8% improvement on the horizontal eye-opening while providing almost the same eye height. It also improves CDR jitter performance by 19%.

TABLE I
COMPARISON BETWEEN CONVENTIONAL AND PROPOSED DFE

	Conventional	**Proposed**	**Improvement**
Number of Taps	5	5	-
Vertical Eye Opening (mV)	61.8	61.1	-1%
Horizontal Eye Opening (ps)	158.2 (0.78UI)	170.7 (0.85UI)	8%
Edge ISI (ps)	41.8 (0.22UI)	29.3 (0.15UI)	30%
CDR Jitter (ps)	20.5 (0.1UI)	16.6 (0.08UI)	19%

IV. CONCLUSION

In this paper, a novel 5-tap half-rate DFE is proposed. The proposed DFE cancels ISIs at both data center and edge simultaneously without using multiple equalizers. Due to efficient reduction of edge ISI, the proposed DFE can help improve the jitter performance of a CDR.

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