RECENT ADVANCES in CIRCUITS

Proceedings of the 19th International Conference on Circuits
(part of CSCC '15)

Zakynthos Island, Greece
July 16-20, 2015

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Plenary Lecture 1

Error Estimation in the Decoupling of Ill-Defined and/or Perturbed Nonlinear Processes

Professor Pierre Borne (IEEE Fellow)
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Abstract: This lecture deals with the definition of the attractors characterizing the precision of decoupling control laws for a nonlinear process in presence of uncertainties and/or bounded perturbations. This approach is based on the use of aggregation techniques and the definition of a comparison system of the controlled process.

Brief Biography of the Speaker: Pierre BORNE received the Master degree of Physics in 1967 and the Master of Electrical Engineering, the Master of Mechanics and the Master of Applied Mathematics in 1968. The same year he obtained the Diploma of "Ingenieur IDN" (French "Grande Ecole"). He obtained the PhD in Automatic Control of the University of Lille in 1970 and the DSc in physics of the same University in 1976. Dr BORNE is author or co-author of about 200 Publications and book chapters and of about 300 communications in international conferences. He is author of 18 books in Automatic Control, co-author of an english-french, french-english « Systems and Control » dictionary and co-editor of the "Concise Encyclopedia of Modelling and Simulation" published with Pergamon Press. He is Editor of two book series in French and co-editor of a book series in English. He has been invited speaker for 40 plenary lectures or tutorials in International Conferences. He has been supervisor of 76 PhD Thesis and member of the committee for about 300 doctoral thesis . He has participated to the editorial board of 20 International Journals including the IEEE, SMC Transactions, and of the Concise Subject Encyclopedia . Dr BORNE has organized 15 international conferences and symposia, among them the 12th and the 17 th IMACS World Congresses in 1988 and 2005, the IEEE/SMC Conferences of 1993 (Le Touquet – France) and of 2002 (Hammamet - Tunisia) , the CESA IMACS/IEEE-SMC multiconferences of 1996 (Lille – France) , of 1998 (Hammamet – Tunisia) , of 2003 (Lille-France) and of 2006 (Beijing, China) and the 12th IFAC LSS symposium (Lille France, 2010) He was chairman or co-chairman of the IPCs of 34 international conferences (IEEE, IMACS, IFAC) and member of the IPCs of more than 200 international conferences. He was the editor of many volumes and CDROMs of proceedings of conferences. Dr BORNE has participated to the creation and development of two groups of research and two doctoral formations (in Casablanca, Morocco and in Tunis, Tunisia). twenty of his previous PhD students are now full Professors (in France, Morocco, Tunisia, and Poland). In the IEEE/SMC Society Dr BORNE has been AdCom member (1991-1993 ; 1996-1998), Vice President for membership

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(1992-1993) and Vice President for conferences and meetings (1994-1995, 1998-1999). He has been associate editor of the IEEE Transactions on Systems Man and Cybernetics (1992-2001). Founder of the SMC Technical committee « Mathematical Modelling » he has been president of this committee from 1993 to 1997 and has been president of the « System area » SMC committee from 1997 to 2000. He has been President of the SMC Society in 2000 and 2001, President of the SMC-nomination committee in 2002 and 2003 and President of the SMC-Awards and Fellows committee in 2004 and 2005. He is member of the Advisory Board of the "IEEE Systems Journal" . Dr. Borne received in 1994, 1998 and 2002 Outstanding Awards from the IEEE/SMC Society and has been nominated IEEE Fellow the first of January 1996. He received the Norbert Wiener Award from IEEE/SMC in 1998, the Third Millennium Medal of IEEE in 2000 and the IEEE/SMC Joseph G. Wohl Outstanding Career Award in 2003. He has been vice president of the "IEEE France Section" (2002-2010) and is president of this section since 2011. He has been appointed in 2007 representative of the Division 10 of IEEE for the Region 8 Chapter Coordination sub-committee (2007-2008) He has been member of the IEEE Fellows Committee (2008- 2010) Dr BORNE has been IMACS Vice President (1988-1994). He has been co-chairman of the IMACS Technical Committee on "Robotics and Control Systems" from 1988 to 2005 and in August 1997 he has been nominated Honorary Member of the IMACS Board of Directors. He is since 2008 vice-president of the IFAC technical committee on Large Scale Systems. Dr BORNE is Professor "de Classe Exceptionnelle" at the "Ecole Centrale de Lille" where he has been Head of Research from 1982 to 2005 and Head of the Automatic Control Department from 1982 to 2009. His activities concern automatic control and robust control including implementation of soft computing techniques and applications to large scale and manufacturing systems. He was the principal investigator of many contracts of research with industry and army (for more than three millions €) Dr BORNE is "Commandeur dans l'Ordre des Palmes Acad?miques" since 2007. He obtained in 1994 the french " Kulman Prize". Since 1996, he is Fellow of the Russian Academy of Non-Linear Sciences and Permanent Guest Professor of the Tianjin University (China). In July 1997, he has been nominated at the "Tunisian National Order of Merit in Education" by the Republic of Tunisia. In June 1999 he has been nominated « Professor Honoris Causa » of the National Institute of Electronics and Mathematics of Moscow (Russia) and Doctor Honoris Causa of the same Institute in October 1999. In 2006 he has been nominated Doctor Honoris Causa of the University of Waterloo (Canada) and in 2007 Doctor Honoris Causa of the Polytechnic University of Bucharest (Romania). He is "Honorary Member of the Senate" of the AGORA University of Romania since May 2008 He has been Vice President of the SEE (French Society of Electrical and Electronics Engineers) from 2000 to 2006 in charge of the technical committees. He his the director of publication of the SEE electronic Journal e-STA and chair the publication committee of the REE Dr BORNE has been Member of the CNU (French National Council of Universities, in charge of nominations and promotions of French Professors and Associate Professors) 1976-1979, 1992-1999, 2004-2007 He has been Director of the French Group of Research (GDR) of the CNRS in Automatic Control from 2002 to 2005 and of a "plan pluriformations" from 2006 to 2009. Dr BORNE has been member of the Multidisciplinary Assessment Committee of the "Canada Foundation for Innovation" in 2004 and 2009. He has been referee for the nominations of 24 professors in USA and Singapore. He is listed in the "Who is Who in the World" since 1999.

Plenary Lecture 2

Applications of Linear Algebra in Signal Processing, Wireless Communications and Bioinformatics

Professor Erchin Serpedin
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Abstract: In this talk, we will review some of the most important applications of linear algebra in signal processing, wireless communications and bioinformatics, and then outline some of the major open problems which might benefit by the usage of linear algebra concepts and tools.

Brief Biography of the Speaker: Dr. Erchin Serpedin is currently a professor in the Department of Electrical and Computer Engineering at Texas A&M University in College Station. He is the author of 2 research monographs, 1 textbook, 9 book chapters, 105 journal papers and 175 conference papers. Dr. Serpedin serves currently as associate editor for the Physical Communications Journal (Elsevier) and EURASIP Journal on Advances in Signal Processing, and as Editor-in-Chief of the journal EURASIP Journal on Bioinformatics and Systems Biology edited by Springer. He is an IEEE Fellow and his research interests include signal processing, biomedical engineering, bioinformatics, and machine learning.

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Plenary Lecture 3

Reliability Life Cycle Management for Engineered Systems

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Abstract: Engineered systems are becoming more complex and by necessity more unreliable resulting in detrimental events for the system itself and its operator. There is evidence to support the contention that industrial and manufacturing processes, transportation and aerospace systems, among many others, are subjected to severe stresses, external and internal, that contribute to increased cost, operator workload, frequent and catastrophic mishaps that require the development and application of new and innovative technologies to improve system reliability, safety, availability and maintainability. These requirements are not true only for strictly engineered systems but are often discussed in business and finance, biological systems and social networks. We introduce in this talk a systematic and verifiable methodology to improve system reliability, reduce operating costs and optimize system design or maintenance practices. The enabling technologies build upon modeling tools to represent critical system functions, a prognostic strategy to predict the long-term behavior of systems under stress, reliability analysis methods exploiting concepts of probabilistic design and an optimization algorithm to arrive at optimum system design for improved reliability. We demonstrate the efficacy of the approach with examples from the engineering domain.

Brief Biography of the Speaker: Dr. George Vachtsevanos is currently serving as Professor Emeritus at the Georgia Institute of Technology. He served as Professor of Electrical and Computer Engineering at the Georgia Institute of Technology from 1984 until September, 2007. Dr Vachtsevanos directs at Georgia Tech the Intelligent Control Systems laboratory where faculty and students began research in diagnostics in 1985 with a series of projects in collaboration with Boeing Aerospace Company funded by NASA and aimed at the development of fuzzy logic based algorithms for fault diagnosis and control of major space station subsystems. His work in Unmanned Aerial Vehicles dates back to 1994 with major projects funded by the U.S. Army and DARPA. He has served as the Co-PI for DARPA's Software Enabled Control program over the past six years and directed the development and flight testing of novel fault-tolerant control algorithms for Unmanned Aerial Vehicles. He has represented Georgia Tech at DARPA's HURT program where multiple UAVs performed surveillance, reconnaissance and tracking missions in an urban environment. Under AFOSR sponsorship, the Impact/Georgia Team is developing a biologically-inspired micro aerial vehicle. His research work has been supported over the years by ONR, NSWC, the MURI Integrated Diagnostic program at Georgia Tech, the U,S. Army's Advanced Diagnostic program, General Dynamics, General Motors Corporation, the Academic Consortium for Aging Aircraft program, the U.S. Air Force Space Command, Bell Helicopter, Fairchild Controls, among others. He has published over 300 technical papers and is the recipient of the 2002-2003 Georgia Tech School of ECE Distinguished Professor Award and the 2003-2004 Georgia Institute of Technology Outstanding Interdisciplinary Activities Award. He is the lead author of a book on Intelligent Fault Diagnosis and Prognosis for Engineering Systems published by Wiley in 2006.

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Plenary Lecture 4

Augmented Reality: The Emerging Trend in Education

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Abstract: Augmented Reality (AR) is the layering of virtual information over the real, 3-D world to produce a blended reality. AR has been considered a significant tool in education for many years. It adds new layers of interactivity, context, and information for learners which can deepen and enrich the learning experience. The combination of real and virtual allows the student to engage in learning about a topic from multiple perspectives and data sources at levels that are not always available in traditional classroom settings and interactions.
As the usage of mobile devices in formal settings continues to rise, so does the opportunity to harness the power of augmented reality (AR) to enhance teaching and learning. Many educators have experimented with AR, but has it proven to improve what students grasp and retain? Is AR just another fun way to engage students, with little transformation of learning? This plenary speaking will introduce augmented reality as an emerging trend in education, provide an overview of its current development, explore examples of curriculum integration, and also suggest approaches for success.

Brief Biography of the Speaker: Dr. Minjuan Wang (Professor of San Diego State University; Distinguished Research Professor of Shanghai International Studies University)
Homepage: http://www.tinyurl.com/minjuan
Minjuan is Professor of Learning, Design, and Technology at San Diego State University (California, USA), and distinguished professor of Shanghai International Studies University (Shanghai, China). She was recently selected as the "Oriental Scholar" by the Municipal Educational Committee of Shanghai). In addition, she and her American colleagues obtained a four-year 1.3 million grant to study environment protection (including the Golden monkeys) in Fanjingshan, Guizhou province.
Minjuan's work has been highly interdisciplinary, covering the field of education, technology, computer science, geography, and communication. In her 14 years at SDSU, she teaches Designing and Developing Learning for the Global Audience, Mobile Learning Development, Technologies for Course Delivery, and Methods of Inquiry. Her research specialties focus on online learning, mobile learning, Cloud Learning, and intelligent learning (as part of the Intelligent Camps initiative launched by British Telecom). Minjuan is the Editor-in-Chief of a newly established journal-- EAI Transactions on Future Intelligent Educational Environments. She also serves on the editorial boards for four indexed journals: Open Education Research,

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International Journal on E-Learning (IJEL), the Open Education Journal, and Journal of Information Technology Application in Education.

As a winner of several research awards, Minjuan is recognized as one of the high impact authors in blended and mobile learning. She has more than 80 peer-reviewed articles published in indexed journals, such as Educational Technology Research and Development, IEEE Transactions on Education, and British Journal of Educational Technology. She was a keynote and invited speaker to 11 international conferences. In addition, she is also an accomplished creative writer and an amateur flamenco dancer. Her recent Novel--Walking in this Beautiful World—has inspired many young people around the world.

Plenary Lecture 5

Application of Multivariate Empirical Mode Decomposition in EEG Signals for Subject Independent Affective States Classification

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Abstract: Physiological signals, EEG in particular, are inherently noisy and non-linear in nature which are challenging to work with using conventional linear signal processing methods. In this paper, we are adopting a new signal processing method, Multivariate Empirical Mode Decomposition, as a preprocessing method to reconstruct EEG signals according to its instantaneous frequencies. To test its effectiveness, we applied this signal reconstruction technique to analyze EEG signals for a 2-dimensional affect states classification application. To evaluated the proposed EEG signal processing system, a three-class classification experiment were carried out on the “Emobrain” dataset from eNTERFACE'06 with K-nearest neighbors (KNN) and Linear Discriminate Analysis (LDA) as classifiers. A leave-one-subject out cross validation process were used and an averaged correct classification rate of 90.77% were achieved. Another main contribution of this paper was inspired by the growth of non-medical grade EEG headsets and its potential in advanced human-computer interface design. However, to reduce cost and invasiveness, consumer grade EEG headsets have far less number of electrodes. In this paper, we used emotion recognition as a case study, and applied Genetic Algorithm to systematically select the critical channels (or sensor locations) for this application. The results of this study will shed lights on the sensor configuration challenges faced by most consumer-grade EEG headset design projects.

Brief Biography of the Speaker: Konstantinos N. (Kostas) Plataniotis received his B. Eng. degree in Computer Engineering from University of Patras, Greece and his M.S. and Ph.D. degrees in Electrical Engineering from Florida Institute of Technology Melbourne, Florida. He was with the Computer Science Department at Ryerson University, Ontario, Canada from July 1997 to June 1999. Dr. Plataniotis is currently a Professor with The Edward S. Rogers Sr. Department of Electrical and Computer Engineering at the University of Toronto in Toronto, Ontario, Canada, where he directs the Multimedia Laboratory. He is a founding member and the inaugural Director – Research of the Identity, Privacy and Security Institute, IPSI, (www.ipsi.utoronto.ca). Kostas was the Director (January 2010- June 2012) of the Knowledge Media Design Institute, KMDI, (www.kmdi.utoronto.ca) at the University of Toronto.
Dr. Plataniotis was the Guest Editor for the March 2005 IEEE Signal Processing Magazine special issue on “Surveillance Networks and Services”, and the Guest Editor for the EURASIP Applied

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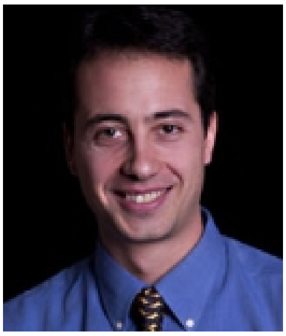
Signal Processing Journal’s special issue on “Advanced Signal Processing & Pattern Recognition Methods for Biometrics”. He is a member of the IEEE Periodicals Review and Advisory Committee (2011-2013); he has served as a member of the 2008 IEEE Educational Activities Board; he chaired of the IEEE EAB Continuing Professional Education Committee, and he served as the 2008 representative of the Computational Intelligence Society to the IEEE Biometrics Council. Dr. Plataniotis chaired the 2009 Examination Committee for the IEEE Certified Biometrics Professional (CBP) Program (www.ieeebiometricscertification.org) and he served on the Nominations Committee for the IEEE Council on Biometrics. He was a member of the Steering Committee for the IEEE Transaction on Mobile Computing, an Associate Editor for the IEEE Signal Processing Letters as well as the IEEE Transactions on Neural Networks and Adaptive Systems and he has served as the Editor-in-Chief for the IEEE Signal Processing Letters from January 1, 2009 to December 31, 2011. Dr. Plataniotis chaired the IEEE Toronto Signal Processing and Applications Toronto Chapter from 2000 to 2002, he was the 2004-05 Chair of the IEEE Toronto Section and a member of the 2006 as well as 2007 IEEE Admissions & Advancement Committees. He served as the Technical Program Committee Co-Chair for the 2013 IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP 2013) and he is the Vice President – Membership for the IEEE Signal Processing Society (2014-2016).
Dr. Plataniotis is a Fellow of IEEE, Fellow of the Engineering Institute of Canada, a registered professional engineer in the province of Ontario, and a member of the Technical Chamber of Greece.
The recipient of numerous grants and research contracts as the principal investigator, he speaks internationally and writes extensively in his field and he has been a consultant to a number of companies. He has served as lecturer in 12 short courses to industry and continuing education programs; he is a contributor to seventeen books, the co-author of “Color Image Processing and Applications”, Springer Verlag, 2000, (ISBN-3-540-66953-1) and “WLAN Positioning Systems: Principles & applications in Location-based Services”, Cambridge University Press, 2012 (ISBN 978-0-521-9185-2), “Multi-linear Subspace Learning: Reduction of multi-dimensional data}, CRC Press, 2013, (ISBN: 978-14398557243). He is the co-editor of “Color Imaging: Methods and Applications”, CRC Press, September 2006, (ISBN 084939774X) and the Guest Editor of the IEEE/Wiley Press volume on “Biometrics: Theory, Methods and Applications” published in October 2009 (ISBN: 9780470247822). Dr. Plataniotis has published more than 400 papers in refereed journals and conference proceedings. In 2005 he became the recipient of the IEEE Canada Engineering Educator Award for “contributions to engineering education and inspirational guidance of graduate students”. Dr. Plataniotis is the joint recipient of the “2006 IEEE Trans. on Neural Networks Outstanding Paper Award” for the published in 2003 “Face recognition using kernel direct discriminant analysis algorithms”, IEEE Trans. on Neural Networks, Vol. 14, No 1, 2003.

Plenary Lecture 6

State of the Art and Recent Progress in Uncertainty Quantification for Electronic Systems (i.e. Variation-Aware or Stochastic Simulation)



Professor Luca Daniel
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Abstract: On-chip and off chip fabrication process variations have become a major concern in today's electronic systems design since they can significantly degrade systems' performance. Existing commercial circuit and MEMS simulators mostly rely on the well known Monte Carlo algorithm in order to predict and quantify such performance degradation. However during the last decade a large variety of more sophisticated and efficient alternative approaches have been proposed to accelerate such critical task. This talk will first review the state of the art of most modern uncertainty quantification techniques including intrusive and sampling-based ones. It will be shown in particular how parameterized model order reduction, and low-rank tensor based representations can be used to accelerate most uncertainty quantification tools and to handle the curse of dimensionality. Examples will be presented including amplifiers, mixers, voltage controlled oscillators with tunable micro-electro-mechanical capacitors and phase locked loops.

Brief Biography of the Speaker: Luca Daniel is an Associate Professor in the Electrical Engineering and Computer Science Department of the Massachusetts Institute of Technology (MIT). Prof. Daniel received the Ph.D. degree in Electrical Engineering from the University of California, Berkeley, in 2003. In 1998, he was with HP Research Labs, Palo Alto. In 2001, he was with Cadence Berkeley Labs.

Dr. Daniel research interests include development of integral equation solvers for very large complex systems, stochastic field solvers for large number of uncertainties, and automatic generation of parameterized stable compact models for linear and nonlinear dynamical systems. Applications of interest include simulation, modeling and optimization for mixed-signal/RF/mm-wave circuits, power electronics, MEMs, nanotechnologies, materials, MRI, and the human cardiovascular system.

Prof. Daniel has received the 1999 IEEE Trans. on Power Electronics best paper award; the 2003 best PhD thesis awards from both the Electrical Engineering and the Applied Math departments at UC Berkeley; the 2003 ACM Outstanding Ph.D. Dissertation Award in Electronic Design Automation; 5 best paper awards in international conferences, 8 additional nominations for best paper award; the 2009 IBM Corporation Faculty Award; and the 2010 IEEE Early Career Award in Electronic Design Automation.

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Distributed power generation using small wind turbine systems: new chaotic attractor in back-to-back converter dynamics

Donato Cafagna and Giuseppe Grassi

***Abstract*—**Referring to distributed power generation, this paper deals with a small wind turbine system (WTS) constituted by a permanent magnet synchronous generator (PMSG) connected to the grid via a back-to-back converter. By considering the behavior of a grid-side converter in the presence of voltage sags, the study shows that a new chaotic attractor is generated when the size of the dc-link capacitor is reduced. The reported time waveforms and state-space attractor clearly highlight that the system becomes chaotic during the voltage sag, being stable before and after the occurrence of the disturbance. Finally, the chaotic behavior is validated via the computation of the maximum Lyapunov exponent, thus confirming the novel phenomenon described herein.

***Keywords*—C**haotic attractors, converters back-to-back, Lyapunov exponents, nonlinear dynamics, wind turbine systems.

I. Introduction

IN the field of renewable energy, great efforts have been recently devoted to distributed generation through small wind turbine systems (WTSs). This choice is motivated by virtue of their higher feed-in tariffs, capability to work in island-mode for isolated communities, national laws imposing simpler grid connection, lower noise level and lower impact on the landscape [1-3]. Over the last years the field of small generation has been mainly dominated by the use of asynchronous generators directly connected to the grid. Very recently, WTSs based on permanent magnet synchronous generators (PMSGs) and back-to-back converters have been introduced [4-5]. The back-to-back converter consists of a PWM (Pulse Width Modulation) rectifier and a PWM inverter connected with a common dc-link. The presence of a fast control loop for the dc-link voltage makes perceive the possibility of reducing the size of the dc-link capacitor, seemingly without affecting the inverter performance [6]. However, since back-to-back converters are rich in nonlinearities, it is important to carefully study their dynamics. Namely, chaotic behaviors may occur in nonlinear dynamical systems, especially in the presence of disturbances [7].

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Note that the large increase in the installed wind capacity necessitates that WTSs remain in operation in the case of the grid disturbances.

Based on these considerations, in this paper the nonlinear dynamics of a grid-side converter is analyzed by reducing the size of the dc-link capacitor in the presence of voltage sags. The conducted analysis shows that a new chaotic attractor is generated for some values of the dc-link capacitance. In particular, the paper reports the time waveforms of the voltage across the capacitor and the grid current in the *d*-axis, showing that chaotic behaviors occur during the voltage sag. Moreover, in order to carefully analyze the conceived phenomena, some attractors are plotted in the state space. These attractors clearly highlight that the system becomes chaotic during the voltage sag, being stable before and after the occurrence of the disturbance. To the best of our knowledge, the results reported herein represent a new finding in the field of small WTSs constituted by PMSGs connected to the grid via back-to-back converters.

The paper is organized as follows. In Section II the overall system and the grid side converter control are described. Section III presents the basic notions on chaos theory, whereas in Section IV chaotic phenomena occurring during voltage sags are analyzed in detail. Finally, the chaotic behavior of the considered small WTS is validated via the computation of the Lyapunov exponents.

II. Wind Turbine System and Grid-side Converter

In small WTS (power unit less than 200 kW) two main choices are available: variable speed asynchronous generators and synchronous generators. Referring to variable speed asynchronous generators, they can easily operate in parallel with large power systems (the utility grid controls voltage and frequency whereas static and reactive compensating capacitors are used for power factor correction and harmonic reduction). On the other hand, over the last years the most common solution for wind generator is based on PMSG directly connected to the turbine [6]. This solution is particularly advantageous as it reduces the frequency and the costs of maintenance operations. In fact these generators are self-excited, allowing operation at high power factor and high efficiency. Moreover multipolar PMSG does not need the gearbox to adapt the rotor speed to the blade speed. This advantage becomes crucial for wind turbine installation in

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harsh environment characterized by low temperature [2]. Figure 1 shows the scheme of a small WTS based on a PMSG.

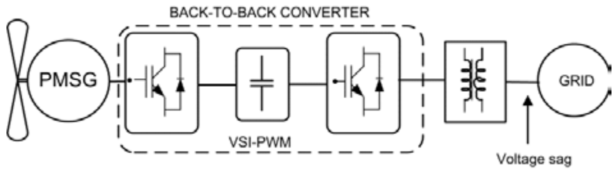

Fig. 1: Wind Turbine System.

The considered PMSG is connected to the grid through a bidirectional converter. It consists of two VSI (Voltage Source Inverter)-PWM converters connected by a storage capacitor: the converter connected to the generator is used as a rectifier, while the converter connected to the grid is used as an inverter. To achieve full control of the output, the dc-link voltage must be boosted to a level higher than the amplitude of the grid voltage [2]. The power flow of the grid side converter is controlled in order to keep the dc-link voltage constant, while the control of the generator side is set to suit the magnetization demand and the reference speed or torque.

A technical advantage of this topology is the capacitor decoupling between the grid converter and the generator converter. This decoupling offers separate control of the two converters, allowing compensation of asymmetry both on the generator side and on the grid side, independently [1]-[3]. Based on the decoupling capability, this paper focuses on the grid side control of the converter, given that the voltage sags occur at the grid side (especially when connected to weak power grids).

Referring to the control scheme of the grid-side converter, its block diagram is shown in Fig. 2. The converter is controlled by two cascade-loops: the outer dc-voltage loop provides the reference for the inner current loop. In particular, the grid-side converter is controlled with a voltage-oriented control (VOC) based on the coordinate transformation between the stationary *α-β* and the synchronous *d-q* reference frames. This control strategy guarantees fast transient response and high static performance due to the internal control loops [8].

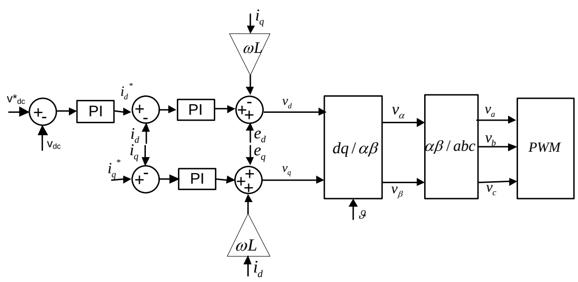

Fig. 2: Grid-side converter control.

The decomposition of the grid current in two axes provides a decoupled control for the active and reactive power and it allows to obtain an high power factor and sinusoidal grid currents [8]-[11]. The active power *P* and the reactive power *Q* produced by WTS are:

$$P = \frac{3}{2}\left(e_d i_d + e_q i_q\right), \quad Q = \frac{3}{2}\left(e_q i_d - e_d i_q\right) \tag{1}$$

If the *dq*-frame has the *d*-axis perfectly aligned on the grid voltage vector, it results $e_q = 0$ and *P* and *Q* become proportional to i_d and i_q, respectively:

$$P = \frac{3}{2} e_d i_d, \quad Q = -\frac{3}{2} e_d i_q \tag{2}$$

indicating that the reactive power flow is controlled via i_q and the dc-link is controlled via i_d. The reference current in the *q*-axis of the current loop is usually set to zero in order to achieve zero phase angle between voltage and current and so unity power factor can be achieved [8].
The grid-side converter control is given by:

$$\begin{cases} v_d^* = v_d + \omega L_{tot} \cdot i_q - e_d \\ v_q^* = v_q - \omega L_{tot} \cdot i_d - e_q \end{cases} \tag{3}$$

The choice of $v*_d$ and $v*_q$ as control variables instead of v_d and v_q lead to decoupling of the dynamics of the *d* and *q* axes. As a consequence the plant of the system is:

$$\begin{cases} i_d = \dfrac{v_d^*}{L_{tot} s + R_{tot}} \\ i_q = \dfrac{v_q^*}{L_{tot} s + R_{tot}} \end{cases} \tag{4}$$

The PI controllers have been tuned with the technical optimum design method. The parameters k_p and T_i are

$$k_p = \frac{L_{tot}}{3T_S}, \quad T_I = \frac{L_{tot}}{R_{tot}} \tag{5}$$

where T_s is the sampling time [2].

III. Chaos Theory Fundamentals

Chaos theory deals with the study of complex behaviors in deterministic nonlinear systems [12]-[16]. In particular, a nonlinear dynamical system is considered to be chaotic if the following three properties hold:

1) *sensitive dependence to initial conditions*;
2) *topological mixing*;
3) *density of periodic orbits.*

Sensitive dependence to initial conditions means that small differences between two sets of initial conditions yield diverging trajectories, rendering long-term prediction impossible to be carried out (an effect usually named “butterfly effect”) [12]. Note that such behavior occurs even though the considered systems are deterministic and no stochastic phenomena are involved.
Topological mixing means that the system will evolve over time so that any given region or open set of its phase space will eventually overlap with any other given region. *Density of periodic orbits* means that every point in the space is approached arbitrarily closely by periodic orbits [12].

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Based on these properties, the trajectories of a chaotic system present the following features [15]:
1) they are not periodic;
2) they are bounded;
3) they cannot be reproduced;
4) they do not intersect each other.

From a practical point of view, a chaotic solution can be identified with a bounded steady-state behavior that is *not* an equilibrium point, *not* periodic, and *not* quasi-periodic. Referring to the time waveform representation, chaotic trajectories behave in a *random-like* fashion. On the other hand, referring to the state-space representation, the complicated geometrical object to which the chaotic trajectories are attracted is called *chaotic attractor* [15].

A key issue in chaos theory is to determine whether the nonlinear dynamical system under consideration is chaotic or non-chaotic. To this purpose, one approach consists in estimating the largest Lyapunov exponent (i.e., a generalization of the eigenvalues at an equilibrium point) from time series data [15]. Since a positive Lyapunov exponent indicates diverging trajectories, what distinguishes chaotic behaviors from non-chaotic ones is the existence of a positive Lyapunov exponent.

IV. New Chaotic Attractor in Back-to-Back Converter Dynamics

It is well known that, due to the non-smooth operation of power electronic converters, back-to-back converters are rich in nonlinearities [7]. As a consequence, it is important to study the nonlinear dynamic behavior of the proposed system, especially in the presence of voltage sags. Based on these considerations, in this Section the nonlinear dynamics of the grid-side converter are analyzed, with the aim to check the existence of some operating conditions for which the system is chaotic. In particular, deep investigation has been devoted to the system configuration in which the capacitance is made small enough, thus allowing the replacement of the commonly used electrolytic capacitors with plastic film capacitors.

Referring to the block diagram reported in Fig.1, a voltage sag is considered at the grid side, which starts at t = 4s with a duration of 0.5s. Owning to the voltage sag, the final voltage is reduced to the 85% of the initial voltage (see Appendix for Low Voltage Ride Through requirements). When the nominal value C = 500μF is considered, the system behaves according to the design specifications as shown in Fig.3, which plots the time waveforms of the voltage V_{dc} across the capacitor (Fig.3 (a)) and the current i_d (Fig.3 (b)). Successively, the system is analyzed by reducing the value of the capacitance. When the value C = 280μF is reached, an interesting nonlinear behavior is found during the voltage sag, that is, the voltage V_{dc} across the capacitor behaves chaotically. Such behavior is clearly shown in Fig.4, which plots the time waveforms of the voltage V_{dc} for different time resolutions.

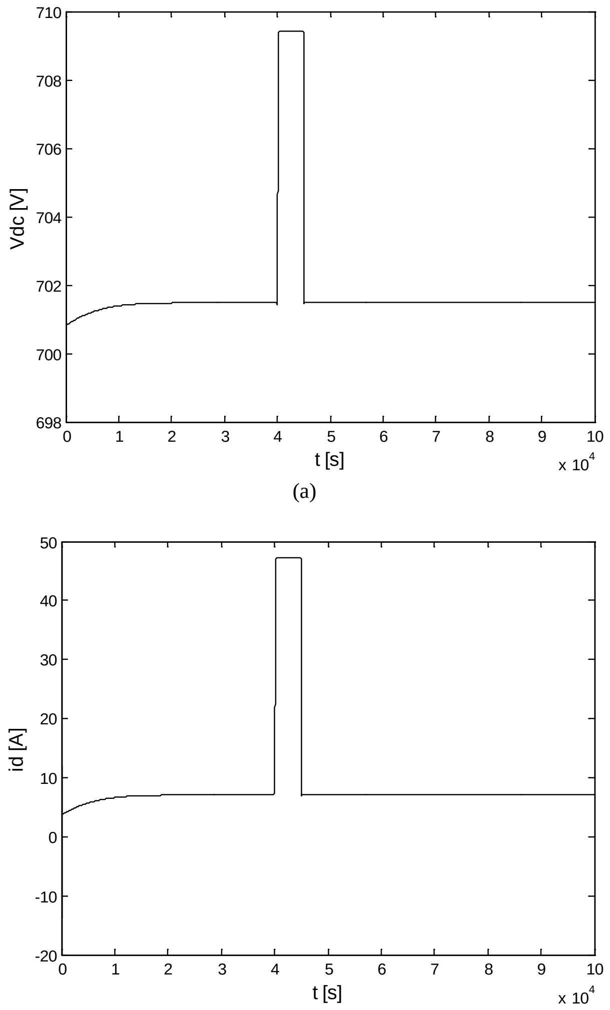

Fig. 3 Time waveforms: (a) voltage V_{dc} across the capacitor; (b) current i_d for C = 500μF.

Notice that the time waveforms of V_{dc} are bounded and not periodic, i.e., they behave in a *random-like* fashion. The same chaotic behavior is found for the current i_d during the voltage sag (see Fig.5).

By plotting the variables V_{dc} and i_d in the state-space, the chaotic attractor depicted in Fig.6 is obtained. In particular, Fig.6(a) shows that the system trajectories start from the initial stable state (701.5V, 7.1A) that exists before the occurrence of the voltage sag. Then the system trajectories approach the one-scroll chaotic attractor reported in Fig.6(b). When the voltage sag ends, the system trajectories return to the initial stable equilibrium point (Fig.6(c)).

Referring to the grid voltage, its dynamic behavior is reported in Fig.7 (upper subplot). Note that the sinusoidal behavior is preserved during the voltage sag, even though the voltage amplitude reduces to the 85% of the initial value. On the other hand, the amplitude of the grid current increases during the voltage sag, as shown in Fig.7 (lower subplot).

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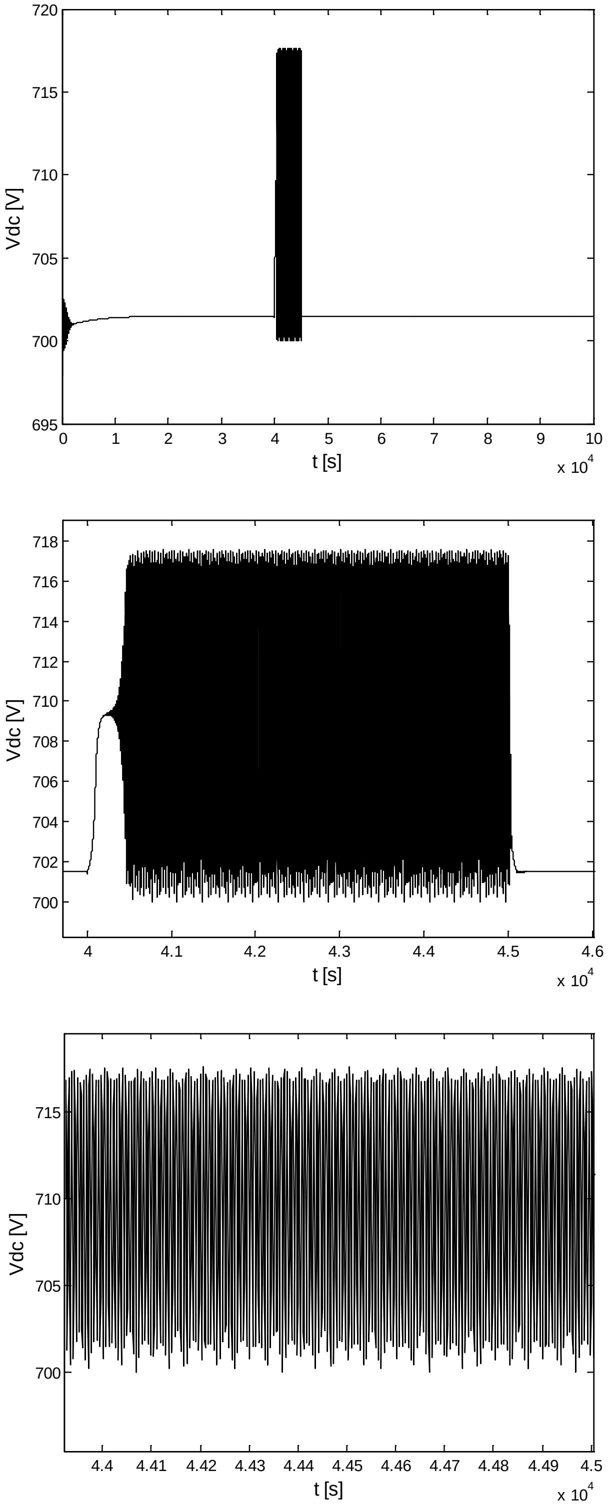


Fig. 4 Time waveforms of the voltage V_{dc} for different time resolutions (C = 280μF).

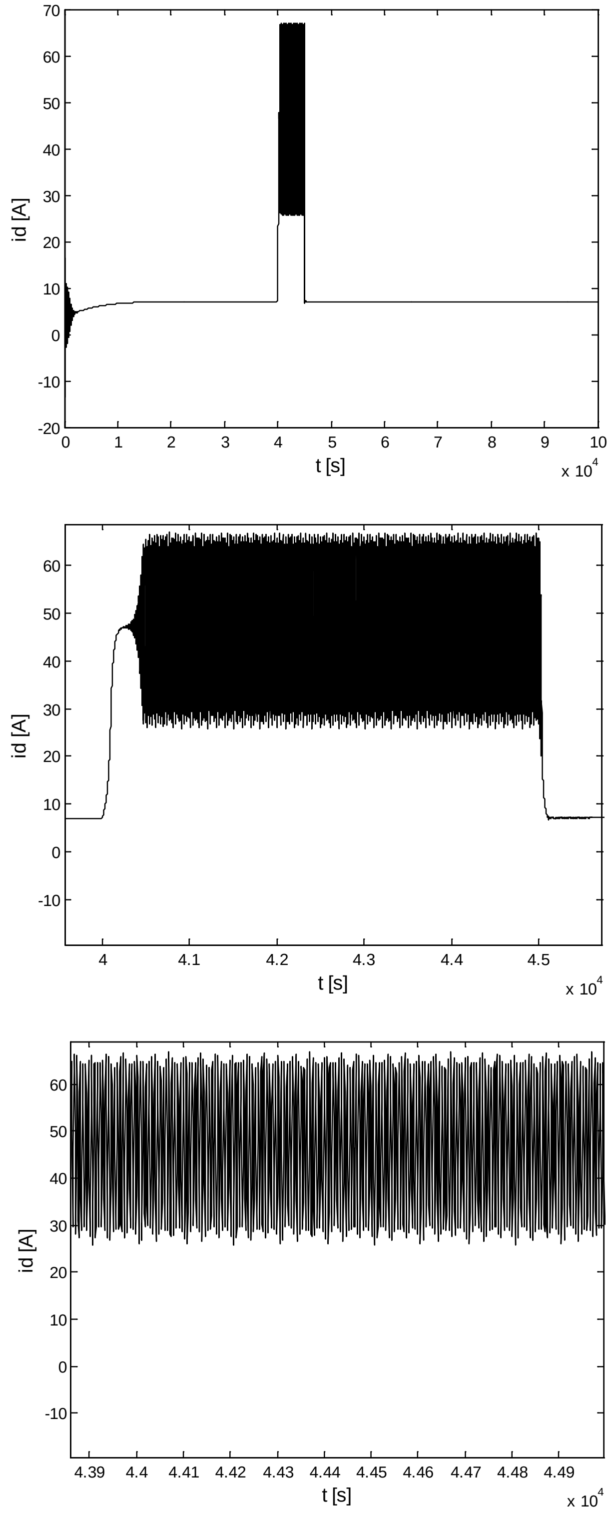
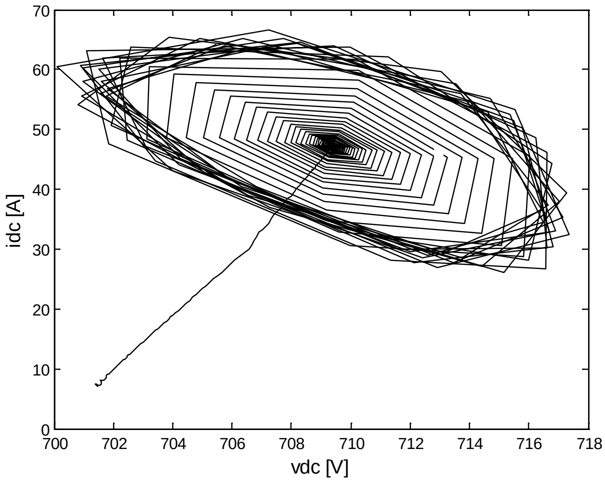
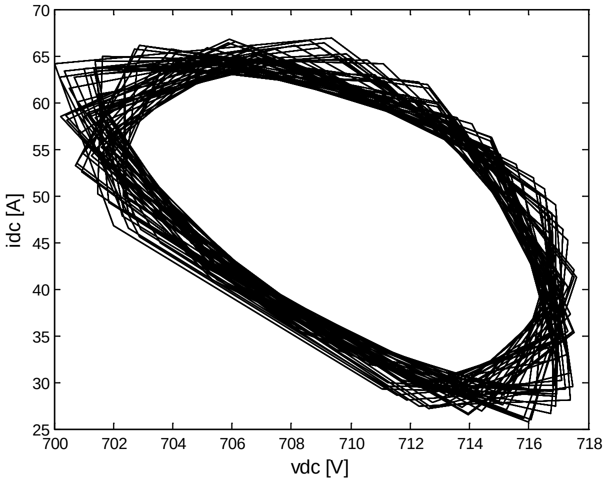


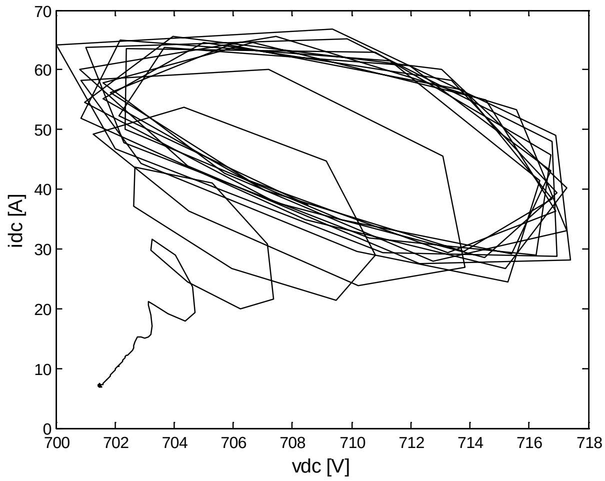
Fig. 5 Time waveforms of the current i_d for different time resolutions (C = 280μF).



(a)



(b)



(c)

Fig. 6 Plots in the state-space (V_{dc}, i_d) for C = 280μF: (a) the trajectories leave the initial stable state (701.5V, 7.1A) that exists before the occurrence of the voltage sag; (b) the trajectories describe a one-scroll chaotic attractor; (c) the trajectories return to the initial stable equilibrium point when the voltage sag ends.

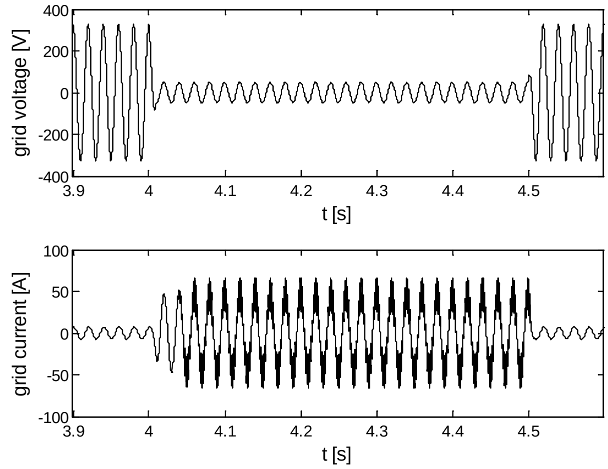


Fig. 7 Time waveforms of the grid voltage and the grid current during the voltage sag (C = 280μF).

In order to verify if the proposed small WTS behaves chaotically for C = 280μF, the maximum Lyapunov exponent has been computed by considering the time series data obtained during the voltage sag. Since the obtained maximum Lyapunov exponent is positive (i.e., λ_{max} = 1.69), it can be concluded that the attractor reported in Fig.6(b) is truly chaotic.

V. Conclusions

The chaotic phenomena occurring during the voltage sag, as described through the paper, represent a new finding for small WTSs constituted by a PMSG connected to the grid via back-to-back converters. In particular, this paper has analyzed the nonlinear dynamics of the grid-side converter in the presence of voltage sags. The study has shown that a new chaotic attractor is generated during the voltage sag when the size of the dc-link capacitor is reduced, being the system stable before and after the occurrence of the disturbance. The chaotic behavior of the considered small WTS has been validated via the computation of maximum Lyapunov exponent.

Appendix

The large increase in the installed wind capacity necessitates that WTS remains in operation in the case of the grid disturbances. For this reason grid codes issued during the last years demand that WTSs must withstand voltage sag to a certain percentage of the nominal voltage and for a specified duration. Such requirements are known as Low Voltage Ride Through (LVRT) [17]. The Italian grid code CEI 0-21 requests that WTS with rated power ≥ 6 kVA must be able not to disconnect instantly during a voltage sag but it must be able to fulfill the LVRT requirements [18]. When the voltage sag occurs, if the WTS is in the region B the WTS shall remain connected to the grid and the active and reactive power injected into the grid can be set to zero. When V ≥ 85% V_{rated} (region A) the system is in normal condition and takes t ≤ 200ms to inject into the grid $P = P_{rated}$ and $Q = Q_{rated}$. In the region C it is possible the disconnection of the system from the grid [18].

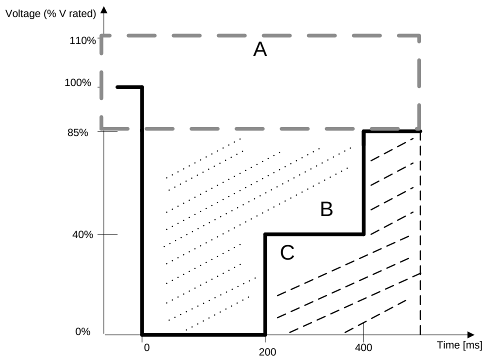


Fig. 8 LVRT requirements.

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High-Impedance Electrode Contact Monitoring

M. J. Burke, C. Molloy, and H. Fossan

Abstract**—**The circuit reported in this paper is used to measure the quality of contact of un-gelled ECG electrodes with the human skin in a heart rate monitor used with mothers prior to and during childbirth. The circuit measures the contact impedance continually and gives an indication of whether the impedance is above or below an acceptable threshold. The output of the circuit is then used to give a visual indication that the mother is adequately connected to the heart-rate monitor for the purposes of obtaining reliable measurements of her heart rate. The output signal obtained is then used to interface with an ultrasonic heart rate transducer being used to measure the unborn infant's heart-rate. This provides a method of ensuring that the ultrasound monitor is actually measuring the infant's heart rate rather than that of the mother. The circuit developed measures the quality of contact of stainless-steel electrodes having contact impedance as high as 100kΩ. It uses an injected signal at a frequency of 5 kHz and can assess the contact of individual left and right electrodes independently.

Keywords**—**Electrode impedance, un-gelled electrodes, heart rate monitoring, ECG amplifier.

I. Introduction

THE Safer Births Program [1], sponsored by the Norwegian Research Council as part of a larger World Health Organization initiative [2], is an action plan aimed at eliminating preventable deaths of infants at birth, with particular focus on developing countries. Many maternity units in these locations are understaffed and in some cases rely on midwives and nurses alone to contend with the complications that arise around birth, without proper access to the advanced medical assistance or equipment needed to deal with them. Few places have sufficient equipment for fetal monitoring such that fetuses in distress are left unattended, adding to the burden of birth asphyxia and stillbirth. Many of the infants born may not be breathing correctly or at all and have pulses which are difficult and sometimes impossible to detect manually. On occasions these infants can be misclassified as stillborn when, in fact, their hearts have not stopped functioning and they could be resuscitated with the help of suitable equipment. Laerdal Medical AS, a Norwegian company that manufactures medical training equipment, is currently extending its range of products to include resuscitation equipment for the scenarios described above. One such product is the Moyo unit shown in Fig 1. This unit is a fetal heart rate monitor which uses an ultrasonic transducer placed on the mother's abdomen to detect the infant's heart beat and indicates the fetal heart rate on a LCD display. One common problem with ultrasonic heart rate monitors is that when the infant's heart beat is difficult to detect the transducer often picks up the mother's heart rate in error [3]. In order to overcome this problem the Moyo unit incorporates an ECG amplifier and circuitry which can be used to measure the mother's heart rate by way of her ECG and to indicate this on a separate LCD display. The Moyo unit is held by the mother giving birth and, when requested to do so, she presses her fingers onto the stainless steel electrodes of the unit which are used to detect her ECG and from this the device measures and displays her heart rate. The values of the two heart rates can then be compared by the midwife and used to discern whether or not the ultrasonic transducer is actually measuring the infant's heart rate reliably or the mother's heart rate in error. To this end it was decided to implement a mechanism in the Moyo unit which would verify that the mother's ECG was being measured reliably by the stainless steel un-gelled electrodes. This is done by measuring the contact impedance of the skin-electrode interface at both electrodes of the Mojo unit and detecting when the mother has pressed her fingers onto the electrodes. The circuit reported in this paper measures the contact impedance of each electrode independently and indicates when the state of contact of either electrode is unsatisfactory for the purposes of reliable ECG measurement, generating a visual alarm under this condition.

Fig. 1. The Handheld Moyo Unit

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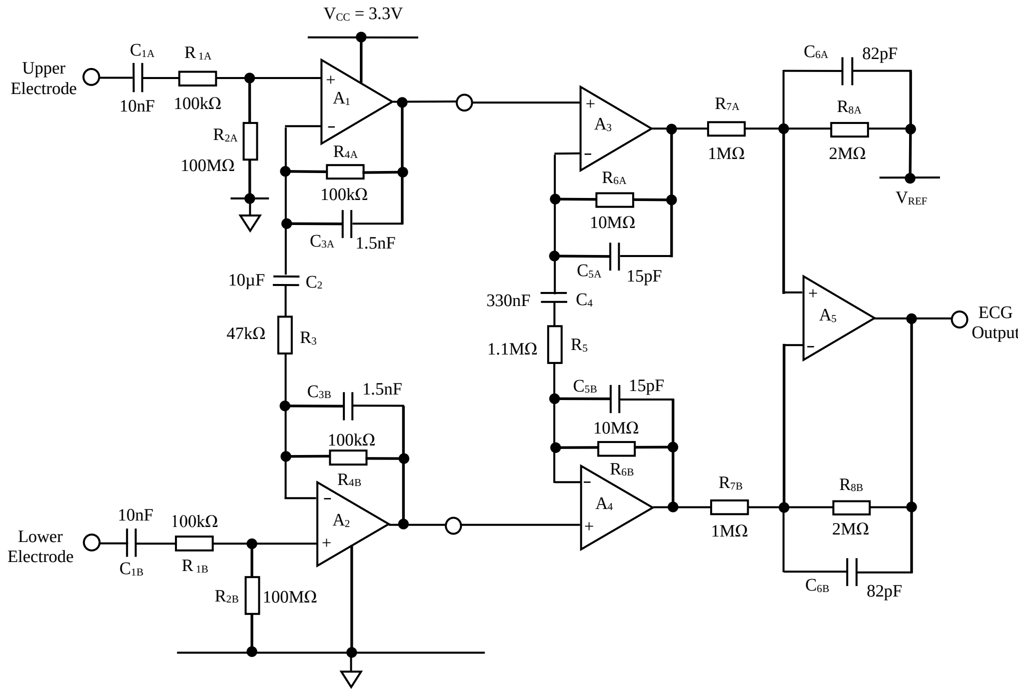

Fig. 2 Schematic Diagram of Existing ECG Amplifier

II. Background

A. *Existing ECG Amplifier*

The schematic diagram of the front-end ECG amplifier currently in use in the Moyo unit is shown in Fig. 2. This is a three-stage instrumentation ECG amplifier adapted from an earlier design by Burke & Gleeson [4,5] and later improved by Assambo & Burke [6-9]. The 46 dB of differential gain is split primarily between the first stage with 14.4 dB and the second stage with 25.6 dB while the third stage provides 6dB of the gain with differential-to-single-ended conversion. The input stage provides a high differential-mode and common-mode impedance of 100MΩ in order to preserve adequate common-mode-rejection-ratio (CMRR) when interfacing with high-impedance dry electrodes. The amplifier operates from a single 3.3V supply rail and the input stages are biased to a mid-rail voltage of 1.65V using a separate dc-to-dc convertor chip not shown in the schematic. The ESD protection elements are also omitted for clarity.

B. *Electrodes*

The electrodes used in the Moyo unit shown in Fig. 1 are made of stainless steel with either a polished or a matt surface, as these can easily be disinfected before use with an alcohol wipe. Electrical contact is made with the electrodes by the mother gripping the unit in both hands with her fingers placed on the electrode surfaces as shown. Only the firmness of the mother's grip determines the contact pressure. In order to obtain an indication of the contact impedance of these electrodes a method formerly reported by Baba & Burke [10, 11] was used to characterize the electrodes. The current source shown in Fig. 3 was used to inject a minute current of 2µA through the electrodes while being held by the user. The current was activated and then deactivated via the relay for stable periods of 20 – 50s. A 10 kHz sinewave signal was also used to allow the high frequency purely resistive components to be evaluated. A program in MATLAB (MathWorks Inc.) was then used to fit a two time constant C-R model shown in Fig. 4 to the recorded voltage waveforms and to determine the values of the individual components of the model.

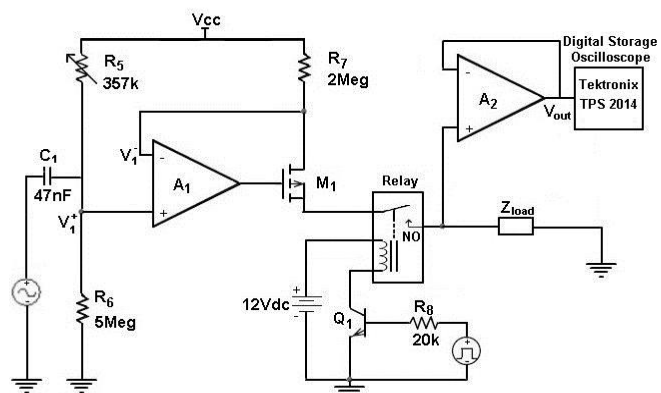

Fig. 3 Electrode Impedance Measurement Circuit

This was done for measurements made on a small number of subjects to get an initial idea of the scale and variation of electrode impedance to be expected. Only the passive components of the model were of interest in this instance and the dc polarization potentials were not measured. The ranges of values measured for each component of the model are listed in Table.1 below. Plots of the magnitude and phase as functions of frequency of a stainless steel electrode having a polished surface are shown in Fig. 5. Plots are shown for light and firm grips of the mother's fingers and for rise and fall phases of the injected current.

Table 1. Range of Values for the Electrode Model Elements

Element	Minimum	Maximum	Unit
$R_1 + R_3$	2.0	5.0	kΩ
R_2	23.2	267	kΩ
C_2	1.60	878	μF
R_4	36.0	380	kΩ
C_4	0.47	55.5	μF
τ_2	0.26	58.8	s
τ_4	0.13	8.62	s

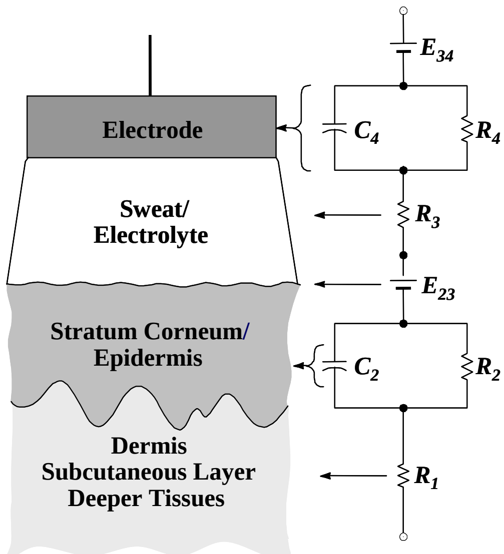

Fig. 4. An Equivalent Electrical Model of the ECG Electrode

It can be seen that the impedance varies considerably within the frequency range of the ECG signal. The magnitude falls off abruptly before 1 Hz and the phase falls off above 10 Hz. It can be seen that the magnitude of the impedance is less than 10 kΩ at frequencies above approximately 10 Hz. This is considerably lower than the input common-mode resistance of the amplifier or the protection resistor, R_1. This indicates that the signal levels involved in measuring the contact impedance of such electrodes are likely to be quite low.

C. *Measurement System*

A block diagram of the electrode contact monitoring system and its placement in relation to the ECG amplifier is shown in Fig. 6. An oscillator and filter are used to provide a sinusoidal source signal at a frequency of 5 kHz with an amplitude of 1.5 V peak. Normally one would like the frequency of contact measurement to be much higher than the bandwidth of the ECG signal. However, the parasitic input capacitance of operational amplifiers causes a significant shunting effect at higher frequencies so the value of 5kHz was chosen to avoid this, while at the same time keeping the measurement frequency at least a decade above the ECG band. The sinewave is then buffered in both an inverting and a non-inverting amplifier to provide antiphase source signals. These signals are then fed through the common-mode input resistors of the ECG amplifier R_{2A} and R_{2B} to the electrode impedances

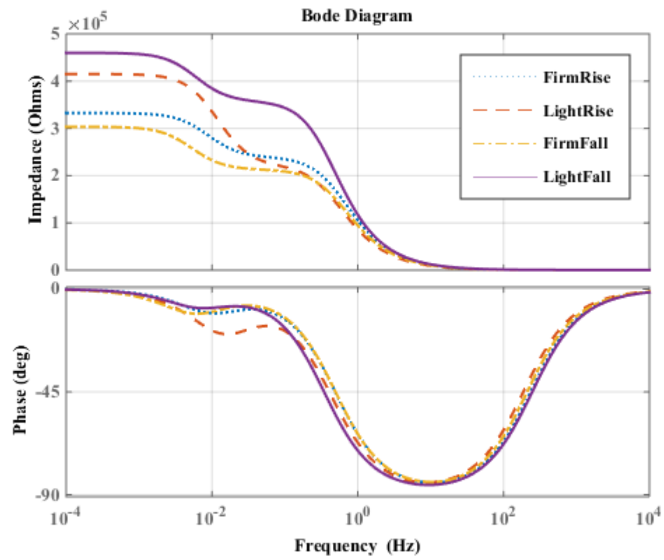

Fig. 5 Impedance of Polished Stainless Steel Electrode

Z_{EA} and Z_{EB}. This method of feeding the contact monitoring signal to the electrodes preserves the high common-mode impedance of the amplifier input and consequently the CMRR. The first stage of the ECG amplifier is also used to provide initial gain for the contact monitoring signal. Band-pass filters centred at 5 kHz are used to extract the contact monitoring signal at the differential outputs of the first stage of the ECG amplifier. The signal at the output of the upper and lower band-pass filters are then fed into half-wave rectifiers on each side so that an indication of the degree of contact of each electrode with the mother's body is obtained. With good contact the signal level detected from each electrode at the input of the ECG amplifier is of the order of 1–2 mV and when amplified and filtered is raised to approximately 500 mV in magnitude. This means that a definitive signal is available to the following pair of threshold detectors for decision making on the quality of electrode contact with the mother's body. Finally the outputs of the threshold detectors are used to drive corresponding LEDs to indicate inadequate contact at either electrode.

D. *Electrode Signal Injection*

The sinewave is then passed through two buffer amplifiers, a non-inverting unity-gain stage built around op-amp A_{10} and a unity-gain inverting stage built around op-amp A_{11}, which also have mid-rail bias voltages. The in-phase component is fed to the upper electrode point via the upper-channel common-mode input resistor R_{2A}. The inverted component is fed to the lower electrode contact point via the lower-channel common-mode resistor R_{2B}. The use of antiphase components allows the signal developed on the mother's body to be kept close to zero.

The levels of 5 kHz signal developed at the input terminals of the ECG amplifier are those developed across the contact impedances of each electrode namely, Z_{EA} and Z_{EB}. With good contact and low skin-electrode impedance the signal levels will be extremely small as the resistor R_2 forms a potential divider with the electrode contact impedance, Z_E, at each

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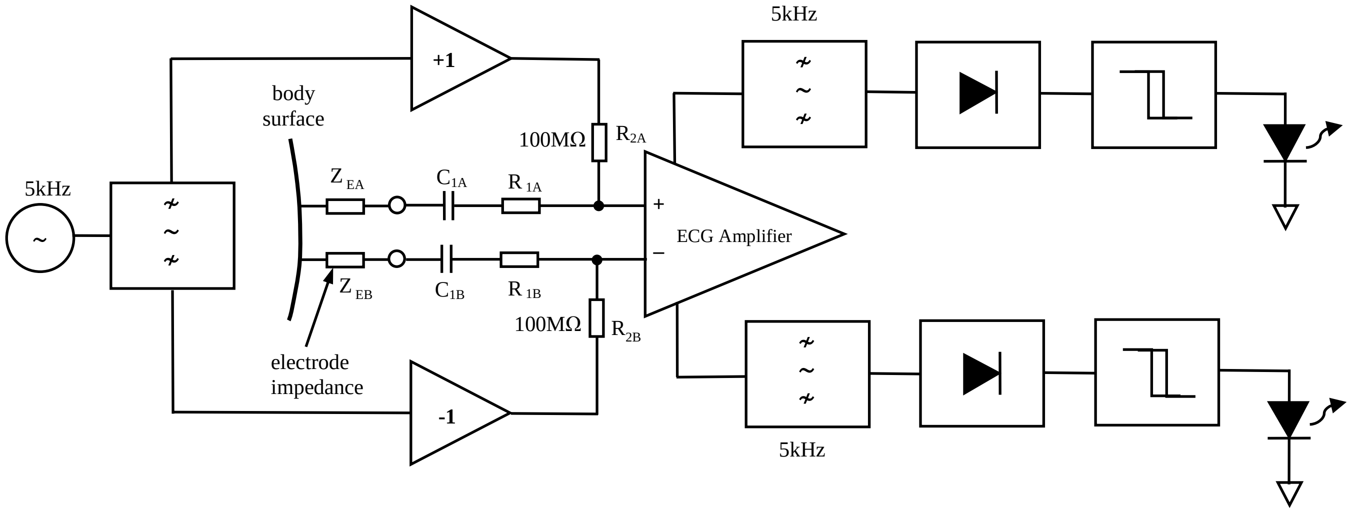

Fig. 6 Block Diagram of the Electrode Contact Monitoring System

terminal of the amplifier. In fact, most of the 5 kHz signal present is actually developed across the protection resistor R_1 in each case. This has a value of 100 kΩ, which is much greater than the contact impedance of the electrode itself. Under normal conditions with good electrode contact the signal at 5 kHz is of the order of 1 mV amplitude. If a maximum electrode contact impedance is set at 200 kΩ, which is twice the typical value of the resistor, R_1, then the maximum expected signal with good electrode contact appearing at the input of the ECG amplifier is then of the order of 3 mV.

E. *ECG Amplifier Revision*

It was decided to use the front-end stage of the ECG amplifier to provide the first phase of amplification for the contact monitoring signal. To this end the gains of the three stages of this amplifier were revised so that the first and second stage gains are now 23 dB and the third stage has unity gain. The revised component values sets the 3 dB lower cut-off frequency at 0.67 Hz as required by the international standards for clinical heart-rate monitoring [12], while at the same time avoiding the use of electrolytic capacitors and increasing the CMRR by 6 dB. The upper cut-off frequency of the first stage was set to 10 kHz while those of the second and third stages are 250 Hz.

F. *Signal Level Detection*

The electrode contact monitoring signals are extracted from the outputs of each side of the first stage of the ECG amplifier using band-pass filters built around op-amps A_{11} and A_{12}. These filters are multiple feedback structures having a centre frequency of 5 kHz, a gain of 26 dB at this frequency and a Q-factor of 20. This provides an overall gain of 49 dB or a factor of 280 to the signal developed across the resistor R_1 and the electrode impedance Z_E in series. The output signal level from the filters with good contact is of then of the order of 150 mV. With poor electrode contact impedance of 200kΩ, this rises to approximately 450 mV peak.

The output sinewave from the band-pass filter channel is then fed into a precision half-wave rectifier in each channel built around op-amps A_{13} and A_{14}. The rectification process is inverting and includes envelope detection of the sinewave by means of a C-R smoothing circuit having a time-constant of 1s. This provides a steady-state level representing the amplitude of the recovered sinewave at 5 kHz. The rectified level is negative-going with respect to the reference voltage of half the supply, V_{REF} = 1.65V. Therefore, at the limit of poor electrode contact, the output voltage of op-amp A_{13} or A_{14} falls to 1.2 V.

Finally, the rectified voltages in each channel are fed into threshold detectors built around op-amps A_{15} and A_{16}. The reference voltage of each threshold detector is set at 1.18 V relative to ground by resistors R_{24} and R_{25} with approximately 50 mV of hysteresis added by the positive feedback provided by resistor R_{26}. The action of the threshold detectors is also inverting. Consequently, when the rectified 5 kHz signal level reaches a threshold of 470 mV below V_{REF} or 1.18 Vdc, the op-amp acting as a comparator changes state and its output goes from 0 V associated with good electrode contact, to the supply voltage of 3.3 V associated with poor electrode contact. This HI output voltage of the op-amp is then used to feed a bipolar transistor based light-emitting-diode (LED) driver that provides a current of 10 mA to the activated LED. This level of current provides sufficient contrast of the light level to allow clear determination the ON/OFF state of the LED.

III. System Verification

Operation of the electrode contact monitoring system was simulated using MultiSim (National Instruments Corp.) The entire schematic of Fig. 7 was entered into the schematic editor. In the first instance the electrodes were modelled as pure resistors. The value of the resistors were varied in non-uniform steps from 1 kΩ to 10 MΩ and the signal level at the output of the filters, V_{A11}, V_{A12}, the half-wave rectifiers, V_{R23A}, V_{R23B} and the threshold detectors, V_{A15}, V_{A16}, were monitored in both upper and lower channels. These levels are shown in Table 2 and can be seen to be a little lower than the design values due to the loading effect of op-amp input capacitance. It can also be seen that the threshold detector logic outputs, change state at a value of electrode resistance

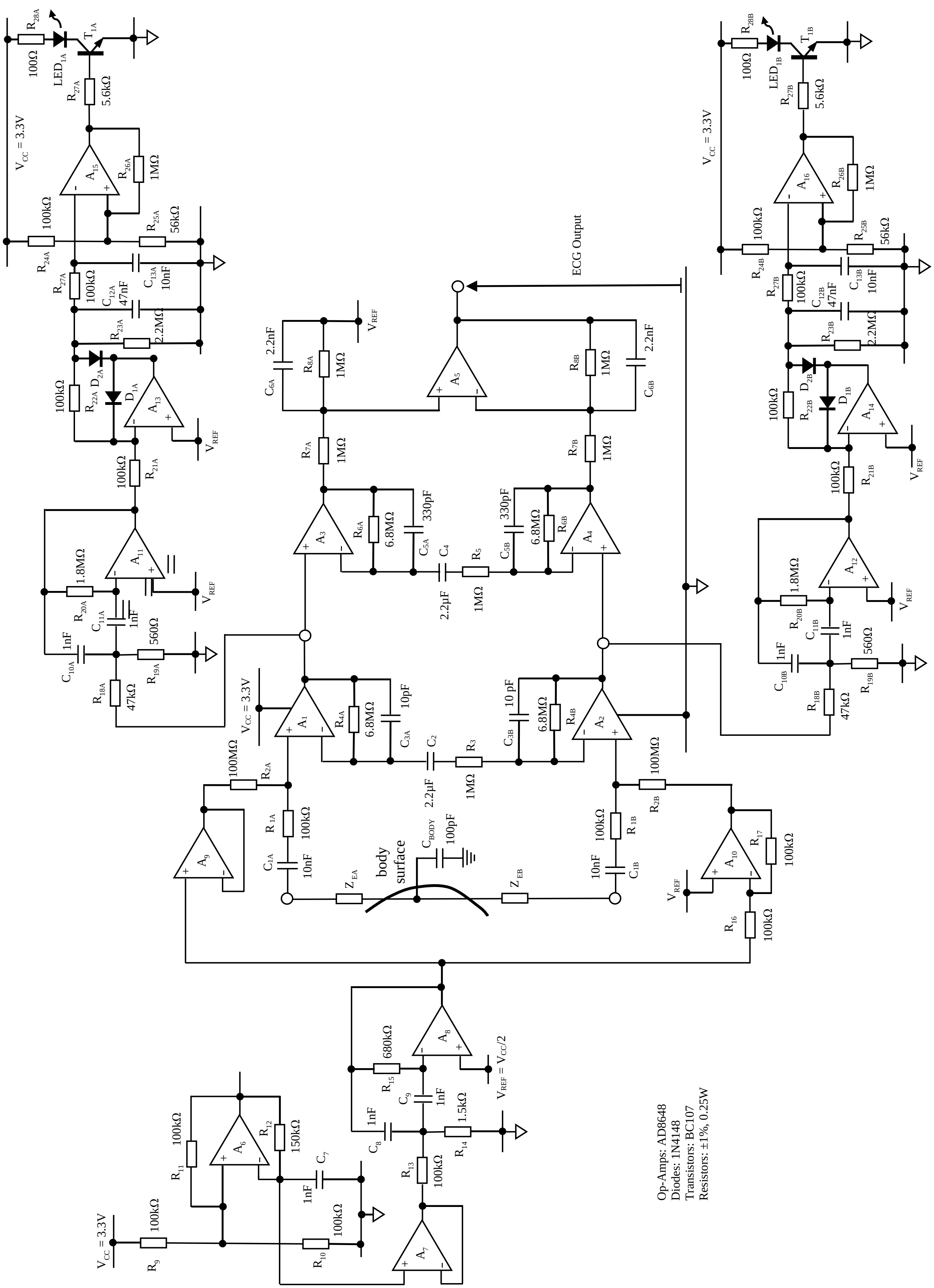

Fig. 7 Schematic Diagram of Electrode Contact Monitor

Table 2 Values of Signal Levels vs Electrode Resistance

$\lvert Z_E \rvert$	V_{A11} (Vpk)	V_{A12} (Vpk)	V_{R23A} (Vdc)	V_{R23B} (Vdc)	V_{A15} (logic)	V_{A16} (logic)
1 kΩ	0.17	0.17	1.49	1.49	LO	LO
2 kΩ	0.17	0.17	1.49	1.49	LO	LO
5 kΩ	0.17	0.17	1.49	1.49	LO	LO
10 kΩ	0.18	0.18	1.48	1.48	LO	LO
20 kΩ	0.19	0.19	1.46	1.46	LO	LO
50 kΩ	0.24	0.24	1.41	1.41	LO	LO
100 kΩ	0.33	0.33	1.34	1.34	LO	LO
200 kΩ	0.48	0.48	1.17	1.17	HI	HI
500 kΩ	0.96	0.96	0.722	0.722	HI	HI
1 MΩ	1.63	1.63	0.519	0.519	HI	HI
2 MΩ	1.65	1.65	0.503	0.503	HI	HI
5 MΩ	1.65	1.65	0.503	0.503	HI	HI
10 MΩ	1.65	1.65	0.501	0.501	HI	HI

between 100 kΩ and 200 kΩ which is considered acceptable. As a more practical test, a set of electrode models identical to that of Fig. 4 were created with the component values measured during the tests outlined in Section II B. This gave 24 electrode models with different component values as given in Table 3. All of the electrode models have good electrode contact as indicated by the output logic states of the threshold detectors. The resistors R_{EA} and R_{EB} are the values of additional resistance which was added in series with the electrodes to cause the respective threshold detectors to change state and activate the LEDs. All of these values are in the region of 100kΩ – 120kΩ. These resistance values were established independently for the two channels indicating that they are very closely matched. This verifies the design functionality of the circuit from the simulation point of view. A hardware prototype is currently under development and will be subjected to comprehensive bench testing when complete.

Table 3 Values of Signal Levels Recorded for a Range of Electrode Models

No	R_1+R_3 (kΩ)	R_2 (kΩ)	C_2 (μF)	τ_2 (s)	R_4 (kΩ)	C_4 (μF)	τ_4 (s)	V_{A11} (mVpk)	V_{A12} (mVpk)	V_{R23A} (Vdc)	V_{R23B} (Vdc)	V_{A15} (logic)	V_{A16} (logic)	R_{EA} (kΩ)	R_{EB} (kΩ)
1	5	97.0	203	19.7	235	1.98	0.47	0.17	0.17	1.5	1.5	LO	LO	110	110
2	5	94.3	383	36.1	213	1.56	0.33	0.16	0.16	1.5	1.5	LO	LO	110	110
3	4	81.6	164	13.4	83.4	10.9	0.91	0.16	0.16	1.5	1.5	LO	LO	120	120
4	4	95.4	464	42.6	81.3	18.8	1.53	0.16	0.16	1.5	1.5	LO	LO	120	120
5	2	94.3	172	16.2	41.8	11.3	0.47	0.11	0.11	1.55	1.55	LO	LO	110	110
6	2	101	277	28.1	46.5	7.0	0.33	0.11	0.11	1.55	1.55	LO	LO	110	110
7	5	198	84.7	0.17	219	1.85	0.41	0.16	0.16	1.5	1.5	LO	LO	120	120
8	5	104	270	28.1	355	1.49	0.53	0.16	0.16	1.5	1.5	LO	LO	120	120
9	4	93.6	254	23.8	63.7	17.7	1.13	0.16	0.16	1.5	1.5	LO	LO	120	120
10	4	106	470	49.8	63.7	21.9	1.40	0.16	0.16	1.5	1.5	LO	LO	120	120
11	2	111	10.5	11.7	43.3	7.51	0.33	0.11	0.11	1.55	1.55	LO	LO	110	110
12	2	111	217	24.1	46.8	7.50	0.35	0.11	0.11	1.55	1.55	LO	LO	110	110
13	5	59.3	116	6.9	132	20.3	2.67	0.16	0.16	1.5	1.5	LO	LO	120	120
14	5	55.7	336	18.7	162	2.36	0.38	0.16	0.16	1.5	1.5	LO	LO	120	120
15	4	79.1	381	30.1	142	6.27	0.89	0.16	0.16	1.5	1.5	LO	LO	110	110
16	4	45.3	576	26.1	124	4.96	0.62	0.16	0.16	1.5	1.5	LO	LO	110	110
17	2	44.5	541	24.1	43.2	6.39	0.28	0.11	0.11	1.55	1.55	LO	LO	120	120
18	2	32.1	784	25.2	61.4	6.29	0.39	0.11	0.11	1.55	1.55	LO	LO	120	120
19	5	144	116	16.7	247	1.49	0.37	0.16	0.16	1.5	1.5	LO	LO	120	120
20	5	67.8	201	13.6	227	2.21	0.50	0.16	0.16	1.5	1.5	LO	LO	110	110
21	4	41.6	504	21.0	64.8	8.2	0.53	0.16	0.16	1.5	1.5	LO	LO	110	110
22	4	42.3	590	24.9	66.8	11.0	0.74	0.16	0.16	1.5	1.5	LO	LO	120	120
23	2	43.8	753	33.0	50.7	14.5	0.74	0.11	0.11	1.55	1.55	LO	LO	110	110
24	2	33.6	633	21.3	49.5	10.5	0.52	0.11	0.11	1.55	1.55	LO	LO	110	110

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Adaptive Control of Temperature inside Plug-flow Chemical Reactor with Pole-placement method and LQ Approach

Jiri Vojtesek, Petr Dostal

***Abstract*—** The tubular chemical reactor is typical nonlinear equipment used in the industry for production of various chemicals. The mathematical description of this kind of system is very complex consisting of partial differential equations. The control strategy used here for controlling of the reactant's temperature by the changes of volumetric flow rate of the coolant in the jacket uses the adaptive approach where controlled nonlinear system is described by the external linear model parameters of which are identified recursively during the control. The control synthesis employs polynomial approach which produces not only the structure of the controller but also relations for computing of controller's parameters. Two modifications of the adaptive control with Pole-placement method and LQ approach are described and discussed in this work.

***Keywords*—**Adaptive Control, Pole-placement Method, Recursive Identification, LQ Approach, Tubular Chemical Reactor.

I. Introduction

THE controlling of chemical reactors is always challenging because of the complexity of the system, hazardous and cost savings. The modeling of such processes usually ends with the complicated set of ordinary or even partial differential equations depending on the type of system [1].

The tubular plug-flow reactor belongs to the ring of systems with continuously distributed parameters, mathematical model of which uses partial differential equations (PDE) unfortunately in the nonlinear form [2].

The mathematical solution of the set of PDE uses Finite differences method which discretize the equation in the axial variable which means that the set of PDE is transformed into the set of ordinary differential equations ODE that can be then solved for example by Runge-Kutta's method [3] which is easily programmable or even build-in function in mathematical software.

Once we have done the simulation of the steady-state and dynamic behavior, we can continue with the choice of the optimal control strategy. There are several let's say "modern" control methods which were tested on this or similar types of systems – the robust control, the predictive control or the adaptive control.

The adaptive control [4] has various improvements and applications. The approach applied in this work uses results from the dynamic analysis for the choice of the External Linear Model (ELM) parameters of which are estimated recursively during the control which satisfies adaptivity of the controller [5].

Control synthesis uses a polynomial approach [6] which satisfies basic control requirements like stability of the control loop, the reference signal tracking and the disturbance attenuation. Another big advantage of this method is that it provides not only the structure of the controller but also relations for computing of the controller's parameters. This method could uses also other methods like the Pole-placement method [6] and LQ approach. These two methods are discussed in this work.

All experiments in the work are done by simulations using mathematical software Matlab, version 7.0.1. These methods were tested and can be used also for the controlling of real systems.

II. Model of Tubular Chemical Reactor

The system under the consideration is a tubular chemical reactor [7] as typical nonlinear equipment used in industry. The reaction inside is a simple exothermic reaction in the liquid phase and the reactant is cooled by the cooling liquid inside the jacket of the reactor. The scheme of the reactor could be found in Fig. 1.

The convection of the liquids in the pipes and the cooling jacket is expected to be plug-flow. That is why are these types of reactors called Plug-Flow Reactors (PFR). The mathematical model uses material and heat balances inside the reactor.

The PFR displayed in Fig. offers theoretically two types of cooling from the direction point of view – co-current and counter-current cooling. It was proofed for example in [8], that the counter-current cooling, where the direction of the cooling flow is opposite to the direction of the reactant has better cooling efficiency. This type of cooling is considered in this work mainly because of this efficiency.

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The mathematical description of such model is very complex and there must be introduced simplifications which reduce the complexity of the system: we expect, that all densities, heat capacities and heat transfer coefficients are expected to be constant. Also, we neglect heat losses and conduction along the metal wall of pipes. On the other hand, the heat transfer through the wall is consequential for the dynamic study. As the space variable is also important in the mathematical description, the mathematical model with all mentioned simplification is described by the set of five partial differential equations (PDE)

$$\begin{aligned}
&\frac{\partial c_A}{\partial t} + v_r \cdot \frac{\partial c_A}{\partial z} = -k_1 \cdot c_A \\
&\frac{\partial c_B}{\partial t} + v_r \cdot \frac{\partial c_B}{\partial z} = k_1 \cdot c_A - k_2 \cdot c_B \\
&\frac{\partial T_r}{\partial t} + v_r \cdot \frac{\partial T_r}{\partial z} = \frac{h_r}{\rho_r \cdot c_{pr}} - \frac{4 \cdot U_1}{d_1 \cdot \rho_r \cdot c_{pr}} \cdot \left(T_r - T_w\right) \\
&\frac{\partial T_w}{\partial t} = \frac{4}{\left(d_2^2 - d_1^2\right) \cdot \rho_w \cdot c_{pw}} \cdot \left[d_1 \cdot U_1 \cdot \left(T_r - T_w\right) + d_2 \cdot U_2 \cdot \left(T_c - T_w\right)\right] \\
&\frac{\partial T_c}{\partial t} - v_c \cdot \frac{\partial T_c}{\partial z} = \frac{4 \cdot n_1 \cdot d_2 \cdot U_2}{\left(d_3^2 - n_1 \cdot d_2^2\right) \cdot \rho_c \cdot c_{pc}} \left(T_w - T_c\right)
\end{aligned} \tag{1}$$

where T denotes temperature, d are diameters of the pipes – d_1 is inner diameter of the pipe, d_2 is outer diameter of the pipe and d_3 denotes diameter of the jacket. Then, ρ are used for densities, c_p for specific heat capacities, U denotes heat transfer coefficients, n_1 is used for number of individual pipes and L is length of the reactor.

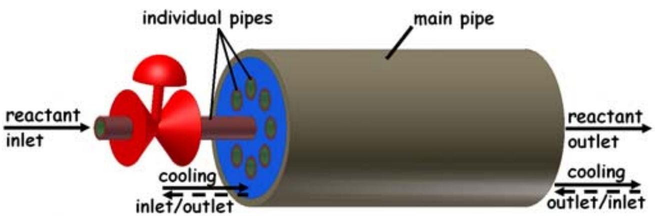

Fig. 1 Scheme of the plug-flow tubular chemical reactor

The variables v_r and v_c are fluid velocities computed from the volumetric flow rate q and constant f, e.g.

$$v_r = \frac{q_r}{f_r}; \quad v_c = \frac{q_c}{f_c} \tag{2}$$

Where constants f_r and f_c are connected to the structure of reactor

$$f_r = n_1 \cdot \frac{\pi \cdot d_1^2}{4}; \quad f_c = \frac{\pi}{4}\left(d_3^2 - n_1 \cdot d_2^2\right) \tag{3}$$

The main nonlinearity of this system can be found in reaction velocities k_1 and k_2 which are nonlinear functions of the rectant's temperature T_r according to the *Arrhenius law*:

$$k_j = k_{0j} \cdot \exp\left(-\frac{E_j}{R \cdot T_r}\right), \text{for } j = 1,2 \tag{4}$$

with k_{0j} as a pre-exponential factors, E_j as a activation energies and R as a universal gas constant.

The last, unmentioned variable in (1) is a reaction heat h_r computed from

$$h_r = h_1 \cdot k_1 \cdot c_A + h_2 \cdot k_2 \cdot c_B \tag{5}$$

where h_j are reaction enthalpies.

Fixed parameters of the reactor [7] are shown in the following Table 1:

Table 1 Fixed parameters of the reactor

$d_1 = 0.02\ m$	$c_{pc} = 4.18\ kJ.kg^{-1}.K^{-1}$
$d_2 = 0.024\ m$	$U_1 = 2.8\ kJ.m^{-2}.K^{-1}.s^{-1}$
$d_3 = 1\ m$	$U_2 = 2.56\ kJ.m^{-2}.K^{-1}.s^{-1}$
$n_1 = 1200$	$k_{10} = 5.61\times10^{16}\ s^{-1}$
$L = 6\ m$	$k_{20} = 1.128\times10^{16}\ s^{-1}$
$q_r = 0.15\ m^3.s^{-1}$	$E_1/R = 13477\ K$
$q_c = 0.275\ m^3.s^{-1}$	$E_2/R = 15290\ K$
$\rho_r = 985\ kg.m^3$	$h_1 = 5.8\times10^4\ kJ.kmol^{-1}$
$\rho_w = 7800\ kg.m^3$	$h_2 = 1.8\times10^4\ kJ.kmol^{-1}$
$\rho_c = 998\ kg.m^3$	$c_{A0}{}^s = 2.85\ kmol.m^{-3}$
$c_{pr} = 4.05\ kJ.kg^{-1}.K^{-1}$	$T_{r0}{}^s = 323\ K$
$c_{pw} = 0.71\ kJ.kg^{-1}.K^{-1}$	$T_{c0}{}^s = 293\ K$

Since the mathematical model of the system (1) is described by the set of nonlinear partial differential equations, we are talking about the *nonlinear distributed-parameters system*.

III. Steady-state and Dynamic Analyses

The static and dynamic analyses are usually the first steps after the modelling part. The goal of these studies is at first verify proposed mathematical model with measurements on the real system. Sometimes simplifications reduce the accuracy of the mathematical description and the use of the mathematical model is unacceptable. The second reason why we do these analyses is that we need to know the behavior of the system for finding of the optimal working point, limitations etc. The step responses in the dynamic analysis are also used for the choice of the External Linear Model in adaptive control described later in this work.

As there are theoretically more input and output variables, the change of the cooling volumetric flow rate, q_c, was chosen as a input variable for the reactant temperature, T_r, as an output variable.

A. Steady-state Analysis

The static analysis explores the behavior of the system in steady-state, i.e. in the state when state variable does not change. Mathematically speaking, the derivatives with respect to time are equal to zero in the steady-state and the set of partial differential equations (1) is transformed to the set of ordinary differential equations with respect to space variable z.

The Finite differences method is employed here for solving of this problem. Derivatives with respect to space variable are replaced by the first back difference

$$\left.\frac{dx}{dz}\right|_{z=z_i} \approx \frac{x(i) - x(i-1)}{h_z}, \text{for } i = 1,2,\dots n \tag{6}$$

with x as a general variable and step size $h_z = L/N_z$. As the system has counter-current cooling, the temperature of the cooling T_c is described in the opposite coordinates and the last fifth equation in (1) uses the first forward difference

$$\left.\frac{dx}{dz}\right|_{z=z_j} \approx \frac{x(j+1)-x(j)}{h_z}, \text{ for } j = n,\ n\text{-}1,\dots 0 \qquad (7)$$

The steady-state analysis is then solution of the cycle of discrete equations for different values of the input variable, in this case volumetric flow rate of the cooling q_c.

The static analysis was done for various values of the cooling volumetric flow rate q_c = <0.1; 0.35> $m^3.s^{-1}$ and values of the steady-state reactant temperature, T_r^s, through the length of the reactor (axial variable z = <0; 8> m) are shown in Fig. 2.

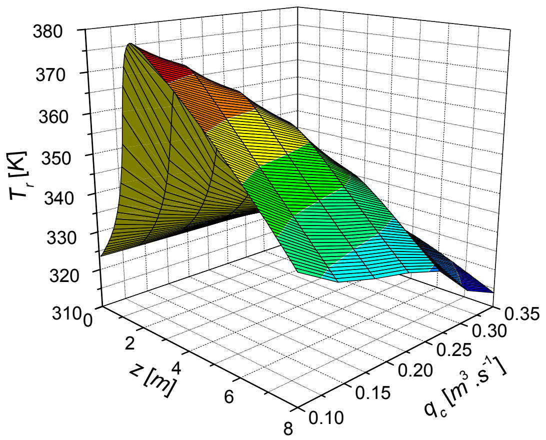

Fig. 2 Steady-state characteristic of the reactant's temperature, T_r, for different volumetric flow rate of the coolant q_c through the length of the reactor

Results of the steady-state analysis clearly show the nonlinearity of the system. The optimal working point is defined for the volumetric flow rate of the reactant q_r^s = 0.150 $m^3.s^{-1}$ and the volumetric flow rate of the coolant q_c^s = 0.275 $m^3.s^{-1}$ and this working point was used later in the dynamic analysis and also in the adaptive control.

B. *Dynamic Analysis*

The dynamic analysis observes the behavior of the output variable, reactant temperature at the end of the reactor $T_r(L)$, after the step change of the input variable, in this case step change of the volumetric flow rate of the coolant, Δq_c. The input, $u(t)$, and the output, $y(t)$ variables for both dynamic and control purposes are then

$$u(t) = \frac{q_c(t)-q_c^s}{q_c^s}\cdot 100[\%]; \quad y(t) = T_r(t,L) - T_r^s(L)[K] \qquad (8)$$

where q_c^s is volumetric flow rate at the working point and $T_r^s(L)$ is the steady-state value of the output variable in the working point which is also initial value for the dynamic study. This means, that the graphs starts from zero.

From the mathematical point of view, the dynamic analysis is the numerical solution of the set of partial differential equations (1). The numerical solution of PDE is not simple and the combination of the Finite differences method described above which transforms the set of PDE to the set of ordinary differential equations (ODE) was used here. The set of ODE is then solved numerically with the use of Runge-Kutta's methods.

There were done several step changes and results are shown in the following Fig. 3.

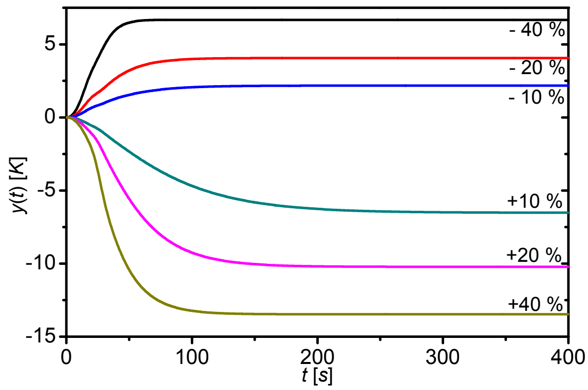

Fig. 3 Dynamic characteristic for various step changes of the input variable

It is clear, that the positive change of the input variable results in decreasing value of the output reactant temperature and conversely, the negative change of q_c produces positive change of the output temperature. All courses of the output variables could be described by second order transfer function which will be used later in the adaptive control.

IV. Adaptive Control

Once we have information about the system's behavior in the steady-state and dynamics, we can move on to the controller design. There are several control methods which can be used for such nonlinear process like predictive control, robust control etc. The adaptive approach was used in this work because authors have good experiences with the usage of this control method for similar types of technological processes like heat exchangers, continuous stirred-tank reactors (CSTR), water tanks etc. An advantage of this method can be also find in the big theoretical background, modifications and applications.

The term "Adaptivity" comes from the nature, where animals and plants *adopt* their behavior depending on the living environment and conditions. Similarly, the adaptive controller could *adopt* (e.g. change) its parameters or structure according to the actual state of the system and control requirements.

There are, of course, various adaptive control strategies. As it is already mentioned, the adaptive approach here is based on on-line recursive identification of the External Linear Model (ELM) which represents original, nonlinear, process. Parameters of the controller depends on parameters of the ELM and changes in every identification step according to the identified parameters of the ELM.

A. External Linear Model

The choice of the ELM comes from the dynamic analysis presented above. The output responses have shown, that the change of the output temperature as the output $y(t)$ to the input variable $u(t)$ in Fig. 3 could be described by the continuous-time (CT) model

$$G(s)=\frac{b(s)}{a(s)}=\frac{b_1 s+b_0}{s^2+a_1 s+a_0} \tag{9}$$

On-line identification of the CT model is complicated. The discrete-time (DT) models are used more often. These models do not describe the system in the very accurate way – it depends on the choice od the sampling period T_v.

Compromise could be found in the use of delta-models as a special type of the DT models where values of the input and output variables are related to the sampling period and it was proofed, that parameters of the delta-model approaches to the parameters of the CT model.

The delta–model introduces a new complex variable γ [9]

$$\gamma=\frac{z-1}{T_v} \tag{10}$$

The ELM (9) could be then rewritten to the form of the differential equation

$$\begin{aligned} y_\delta(k) &= b_0^\delta u_\delta(k-1)+b_1^\delta u_\delta(k-2)-\ldots \\ &\ldots-a_0^\delta y_\delta(k-1)-a_1^\delta y_\delta(k-2) \end{aligned} \tag{11}$$

where b_0^δ, b_1^δ, a_0^δ, a_1^δ are delta-parameters similar to those in (9) for small sampling period [10].

Delta values of input and output variables in Equation (11) can be computed as

$$\begin{aligned} y_\delta(k) &= \frac{y(k)-2y(k-1)+y(k-2)}{T_v^2} \\ y_\delta(k-1) &= \frac{y(k-1)-y(k-2)}{T_v} \qquad u_\delta(k-1)=\frac{u(k-1)-u(k-2)}{T_v} \\ y_\delta(k-2) &= y(k-2) \qquad u_\delta(k-2)=u(k-2) \end{aligned} \tag{12}$$

The regression vector $\boldsymbol{\varphi}_\delta$ and the vector of parameters $\boldsymbol{\theta}_\delta$ are

$$\begin{aligned} \boldsymbol{\varphi}_\delta(k-1) &= \left[-y_\delta(k-1),-y_\delta(k-2),u_\delta(k-1),u_\delta(k-2)\right]^T \\ \boldsymbol{\theta}_\delta(k) &= \left[a_1^\delta,a_0^\delta,b_1^\delta,b_0^\delta\right]^T \end{aligned} \tag{13}$$

and the differential equation (11) has then vector form

$$y_\delta(k)=\boldsymbol{\theta}_\delta^T(k)\cdot\boldsymbol{\varphi}_\delta(k-1)+e(k) \tag{14}$$

where $e(k)$ is a general random immeasurable component and the task of the identification is to estimate the vector of parameters $\boldsymbol{\theta}_\delta$ from known data vector $\boldsymbol{\varphi}_\delta$.

B. Recursive Identification

It was already mentioned, that adaptivity in this approach is based on the on-line parameter identification of the ELM. The recursive identification mathematically means the estimation of the vector of parameters $\boldsymbol{\theta}_\delta$ from the differential equation (14). The method used here is a simple Recursive Least-Squares (RLS) method [11] which can be easily programmed and also extended by the additional "forgetting" techniques. Generally, the RLS method used for estimation of the vector of parameters $\hat{\theta}_\delta^T(k)$ could be described by the set of equations:

$$\begin{aligned} \varepsilon(k) &= y(k)-\boldsymbol{\varphi}^T(k)\cdot\hat{\boldsymbol{\theta}}(k-1) \\ \gamma(k) &= \left[1+\boldsymbol{\varphi}^T(k)\cdot\mathbf{P}(k-1)\cdot\boldsymbol{\varphi}(k)\right]^{-1} \\ \boldsymbol{L}(k) &= \gamma(k)\cdot\mathbf{P}(k-1)\cdot\boldsymbol{\varphi}(k) \\ \mathbf{P}(k) &= \frac{1}{\lambda_1(k-1)}\left[\mathbf{P}(k-1)-\frac{\mathbf{P}(k-1)\cdot\boldsymbol{\varphi}(k)\cdot\boldsymbol{\varphi}^T(k)\cdot\mathbf{P}(k-1)}{\dfrac{\lambda_1(k-1)}{\lambda_2(k-1)}+\boldsymbol{\varphi}^T(k)\cdot\mathbf{P}(k-1)\cdot\boldsymbol{\varphi}(k)}\right] \\ \hat{\boldsymbol{\theta}}(k) &= \hat{\boldsymbol{\theta}}(k-1)+\boldsymbol{L}(k)\varepsilon(k) \end{aligned} \tag{15}$$

where ε denotes a prediction error, $\mathbf{P}$ is a covariance matrix and λ_1 and λ_2 are forgetting factors. For example constant exponential forgetting [11] uses $\lambda_2 = 1$ and

$$\lambda_1(k)=1-K\cdot\gamma(k)\cdot\varepsilon^2(k) \tag{16}$$

where K is a very small value (e.g. $K = 0.001$).

C. Control Synthesis

It was already mentioned, that parameters of the ELM are used in the computation of the controller. The polynomial synthesis is employed here because it provides not only the structure of the controller but also relations for computing of the controller's parameters. Negligible advantage could be found also in the fulfillment of the basic control requirements and easily programmability.

The simplest one degree-of-freedom (1DOF) divides the control loop into two parts – the transfer function $G(s)$ representing controlled plant (i.e. the ELM of the system) and the transfer function of the controller $Q(s)$ – see Fig. 4.

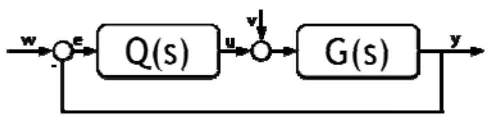

Fig. 4 One degree-of-freedom (1DOF) control configuration

The signal w in Fig. 4 represents reference signal (i.e. wanted value), u is control input, y controlled output, v denotes random error and e is control error – $e = w - y$.

The transfer function of the controlled plant $G(s)$ is known from the recursive identification and the transfer function of the controller is generally

$$\tilde{Q}(s)=\frac{q(s)}{s\cdot\tilde{p}(s)} \tag{17}$$

The parameters of the polynomials $\tilde{p}(s)$ and $q(s)$ are computed from the Diophantine equation

$$a(s)\cdot s\cdot\tilde{p}(s)+b(s)\cdot q(s)=d(s) \tag{18}$$

by the *Method of uncertain coefficients* which compares parameters of individual s-powers in (18). Polynomials $a(s)$ and $b(s)$ are known from the recursive identification and the polynomial $d(s)$ on the right side of the (18) is stable optional polynomial the choice of which affects mainly the quality of the control. Two methods of choosing of this polynomial are discussed and tested in the next chapters – *Pole-placement method* and *LQ approach*.

D. Pole-placement Method

The simplest way is to choose the polynomial $d(s)$ by the Pole-placement method which divides the polynomial generally to

$$d(s) = \prod_{i=1}^{\deg d(s)} (s+\alpha) \quad (19)$$

with the stability condition $\alpha > 0$.

Degrees of polynomials $\tilde{p}(s)$ and $q(s)$ from (17) and the polynomial $d(s)$ in (18) are for this second order transfer function with relative order one (9)

$$\begin{aligned} &\deg \tilde{p}(s) = \deg a(s) - 1 = 1 \\ &\deg q(s) = \deg a(s) = 2 \\ &\deg d(s) = \deg a(s) + \deg \tilde{p}(s) + 1 = 4 \end{aligned} \quad (20)$$

which means that the transfer function of the controller is

$$Q(s) = \frac{q_2 s^2 + q_1 s + q_0}{s \cdot (s + p_0)}, \quad (21)$$

and the polynomial $d(s)$ has four roots. Disadvantage of this method is that there is no rule how to choose there roots. We can have one quadruple root, two double roots, one ordinary and one triple root or four different roots. Our previous experiments have shown that it is good to connect the choice of the polynomial $d(s)$ with the controlled system, for example with the use of spectral factorization of the polynomial $a(s)$ in the numerator of the transfer function $G(s)$.

Let us introduce new polynomial $n(s)$ computed from the spectral factorization of the polynomial $a(s)$, i.e.

$$n^*(s) \cdot n(s) = a^*(s) \cdot a(s) \quad (22)$$

It is clear, that this polynomial has the same degree as the polynomial $a(s)$ and as it is a part of the polynomial $d(s)$, we can rewrite this polynomial to the form

$$d(s) = n(s) \cdot (s+\alpha)^2 \quad (23)$$

which means that we have reduced the uncertainty to one double root.

The controller designed with this method has one tuning parameter – α which could affect the quality of control.

E. LQ Approach

The second, let's say a bit sophisticated, method is for designing of the polynomial $d(s)$ is the use Linear-Quadratic (LQ) approach which is based on the minimization of the cost function

$$J_{LQ} = \int_0^\infty \left\{ \mu_{LQ} \cdot e^2(t) + \varphi_{LQ} \cdot \dot{u}^2(t) \right\} dt \quad (24)$$

in the complex domain. Parameters $\varphi_{LQ} > 0$ and $\mu_{LQ} \geq 0$ are weighting coefficients, $e(t)$ is the control error and $\dot{u}(t)$ denotes the difference of the input variable.

If we use again the spectral factorization of the polynomial $a(s)$, similarly as in previous case, the polynomial $d(s)$ is then divided into

$$d(s) = n(s) \cdot g(s) \quad (25)$$

where the polynomial is solution of the minimization of (24), mathematically solution of the spectral factorization

$$\begin{aligned} (a(s) \cdot f(s))^* \cdot \varphi_{LQ} \cdot a(s) \cdot f(s) + b^*(s) \cdot \mu_{LQ} \cdot b(s) = \ldots \\ \ldots = g^*(s) \cdot g(s) \end{aligned} \quad (26)$$

Degrees of the controller's polynomials $\tilde{p}(s)$ and $q(s)$ and the polynomial $d(s)$ on the right side of Diophantine equation are for the second order ELM (9)

$$\begin{aligned} &\deg \tilde{p}(s) \geq \deg a(s) - 1 = 2 \\ &\deg q(s) = \deg a(s) + \deg f(s) - 1 = 2 \\ &\deg d(s) = 2 \deg a + 1 = 5 \end{aligned} \quad (27)$$

and the transfer function of the controller is

$$Q(s) = \frac{q_2 s^2 + q_1 s + q_0}{s \cdot (s^2 + a_1 s + p_0)} \quad (28)$$

The LQ adaptive controller has two tuning parameters, weighting factors φ_{LQ} and μ_{LQ} but our experiments have shown that is good to fix one parameter and change only the second one [12].

V. Simulation Results

Both techniques were tested by the simulation on the mathematical model (1). The control output is the change of the input volumetric flow rate of the coolant in % and the controlled output is the change of the output temperature, similarly as it is in (8):

$$u(t) = \frac{q_c(t) - q_c^s}{q_c^s} \cdot 100[\%]; \quad y(t) = T_r(t, L) - T_r^s(L)[K] \quad (29)$$

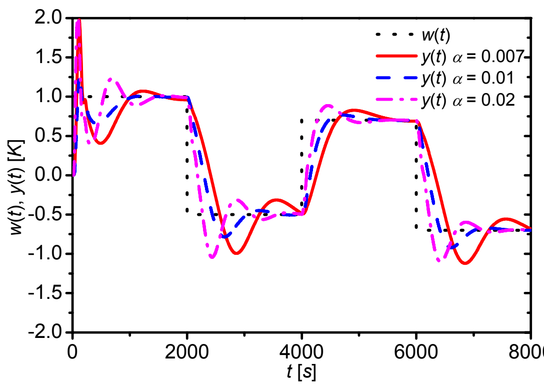

Fig. 5 The course of the reference signal, $w(t)$, and the output variable, $y(t)$, for various values of α, Pole-placement method

Due to better comparability of these methods are also simulation parameters the same. The sampling period was T_v = 1.5 s, the simulation time was 8 000 s and there were done four different step changes to the positive and negative value during this time.

The first control simulation was done for the Pole-placement method and various values of the parameter α. = 0.07; 0.01 and 0.02.

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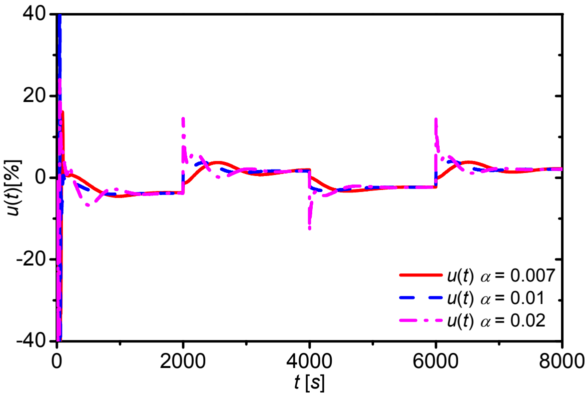

Fig. 6 The course of the input variable, $u(t)$, for various values of α, Pole-placement method

Obtained simulation results in Fig. 5 a 6 have shown that the increasing value of α results in quicker output response but overshoots of the output variable $y(t)$. The course of the control (input) variable $u(t)$ is smoother for lower values of α.

The second analysis was done for LQ approach and different values of weighting parameter ϕ_{LQ} = 0.005; 0.01 and 0.02 and the results are shown in Fig. 7 and 8.

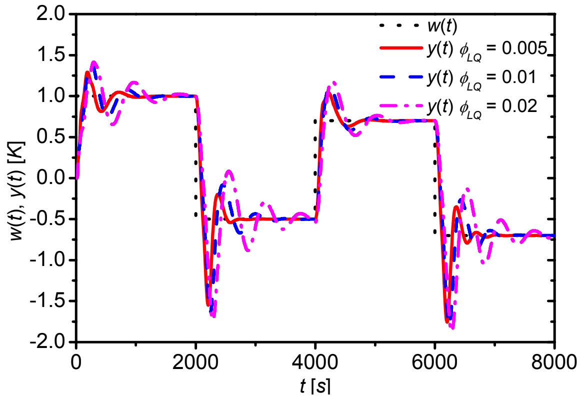

Fig. 7 The course of the reference signal, $w(t)$, and the output variable, $y(t)$, for various values of ϕ_{LQ}, LQ approach

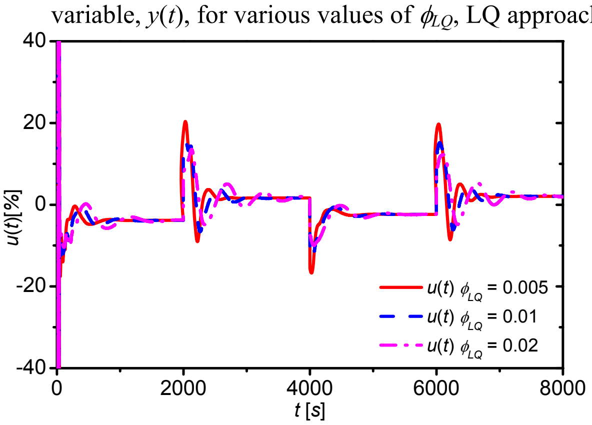

Fig. 8 The course of the input variable, $u(t)$, for various values of ϕ_{LQ}, LQ approach

Although there are similar values of the weighting parameter ϕ_{LQ} as α in previous case, the meaning of this parameter is different. In this case, increasing value of parameter ϕ_{LQ} results in slower, more oscillating output response but smoother course of the input variable which could be sometimes good from the practical point view.

The use of LQ approach produces generally more oscillating output responses but both control techniques could be used for controlling of such strongly nonlinear processes.

VI. Conclusion

The paper presents two modifications of the adaptive control applied on the control of the reactant temperature inside the tubular chemical reactor as a typical nonlinear system with distributed parameters. The nonlinear system is described by the external linear model in the general form parameters of which are estimated recursively during the control which fulfills the "adaptivity" of the system. The difference between these two modifications is in the choice of the stable polynomial in the Diophantine equation. The first method uses simple Pole-placement method with spectral factorization and the second modification is based on the LQ approach again together with the spectral factorization of the polynomial in the denominator of the ELM. Both methods have tuning parameters which can affect the quality of control, mainly the speed of the control and the overshoots. Obtained simulation results have shown the usability of the adaptive control for controlling of such complex nonlinear systems. The future work could be focused on the verification of the obtained results on the real chemical reactor.

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A Methodology for Accurate Defect Tolerance Analysis

Mariem Slimani, Arwa Ben Dhia, and Lirida Naviner

***Abstract*—Yield has been considered as a fundamental criterion in defining a circuit implementation's cost. Thus, more accurate models for defect tolerance analysis are needed to guarantee a good use of fault-tolerant techniques. In this work, we describe a methodology for fault tolerance analysis in combinational circuits. It is a combined transistor-gate level model that uses detection information at the transistor level and the well-known stuck-at fault model at the logic level, to assess the defect tolerance of digital circuits. The model exhibits the same accuracy as transistor-level models, while having a complexity comparable to gate-level ones. Moreover, the proposed methodology is implemented as a simple tool to evaluate the fault tolerance of the circuit. Simulation results for several benchmark circuits demonstrate the accuracy of this tool and its efficiency compared to other defect-tolerant analysis techniques.**

***Index Terms*—Robustness, defect tolerance, defect modeling, transistor-level, gate-level, stuck-at model**

I. Introduction

As feature sizes scale down to the nanometer era, reliability is becoming a serious challenge in nowadays's microelectronics industry [1], [2]. Evaluating the impact of possible faults on the circuit functionality at an early stage of the design flow is highly important to make judicious choices in the design hardening before the fabrication process. Hence, many works have been proposed for reliability analysis [3]–[6]. These works can be classified according to the type of faults, whether they are transient or permanent. Permanent faults, which are the scope of this work, are generally modeled using the stuck-at fault model introduced in [7]. This model is at gate level, where faults affect any structural connections between logic elements. This means basically that intrinsic fault contribution of the circuit gates are not taken into account for defect tolerance estimation. Recently, Mentor Graphics has proposed a transistor-level defect analysis tool called Tessent CellModelGen [8], [9]. This tool has been used in previous works to analyze the defect tolerance of different architectures while considering realistic locations of defects into and outside the circuit gates [10], [11]. Moreover, it considers resistive bridges and opens to take into account the complete analog behaviour of the defect. This tool performs exhaustive analog fault simulation, offering a high accuracy at the expense of long simulation time and memory issues. Our work comes into this scope introducing a new simulation tool for defect tolerance analysis. We propose a methodology to report the detection probability of the circuit, based on a pre-characterization of the detection information of different cells in the library and a gate-level fault simulation. In order to validate the effectiveness of our approach in evaluating the defect tolerance of digital circuits, we compared it first with results from CellModelGen tool for smaller circuits and then with results from SPR and SPR-MP methods for different benchmark circuits [12], [13]. The obtained results clearly show the advantages of the proposed approach, as it allows an exact defect tolerance evaluation, like the SPR-MP method, while allowing the analysis for larger circuits. This paper is organized as follows. Section II presents a brief review of different reliability analysis methods. In Section III, our defect tolerance assessment approach is described on the basis of transistor-gate mixed analysis. Simulation results are discussed in Section IV. Finally, concluding remarks are drawn in Section V.

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II. Defect Tolerance Analysis

Defect tolerance analysis approaches can be classified into two main categories: simulation-based methods and analytical methods.

a) Simulation-based methods: Most of these methods are based on fault injection. It consists in comparing two versions of the circuit, a fault-free version and a fault-prone one, after simulating them under the same conditions (temperature, stimuli, etc). Simulation checks whether the outputs of the faulty version correspond to the correct ones. If so, injected faults did not reach the output and are said to be masked. The ratio between the number of times the faults were not masked and the total number of simulation runs constitutes the detection probability (FR) which is used usually as a metric for defect tolerance assessment. As a matter of fact, faults are injected according to a given model, depending on the granularity of the analysis (at block, gate, or transistor level). Several works do fault injection at gate level model [14], [15]. The drawback of such fault injection is that the faults occurring inside the gates are not taken into account. Thus, for more realistic defect modeling, one should descend at a finer level.

At transistor-level, an industrial study found that in a 130nm fabricated IC design, bridges and opens account for about 58% of all defects [16]. A bridge defect (or short) is an unwanted metal connection between two or more nets. An open defect is a connection break between two nets that should be connected. The short/open model can be applied to connections between transistor terminals and any other net of the circuit. Nevertheless, the most common defect modeling at transistor-level remains the stuck-open and stuck-closed defects [17]. A stuck-open (or stuck-OFF) transistor

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is never conducting, whereas a stuck-closed (or stuck-ON) transistor is always conducting. Recently, Mentor Graphics has proposed a transistor-level defect analysis tool called Tessent CellModelGen [8]. This tool has been used in previous works to analyze the defect tolerance of different architectures while considering realistic locations of faults into and outside the circuit gates [10], [11]. Unfortunately, simulating large circuits with this tool is impossible due to both time and memory issues.

b) Analytical methods: They reduce the circuit into its elementary elements and model its behaviour through formal equations. The Probabilistic Transfer Matrix (PTM) approach, introduced in [18], is among the most known analytical methods. It models each gate in the circuit by a matrix whose elements correspond to the probability that the output of the gate being at logic value '0' or '1' is correct according to the applied input combination. Despite its accuracy, the PTM method suffers from scalability problems. In fact, the PTM of a circuit grows exponentially with the number of inputs and outputs, leading to an intractable computation time and a need for a big storage space in memory, even for medium-sized circuits [19]. Another method based on the PTM matrices, is the Signal Probability Reliability (SPR) method, introduced in [12]. This method outperforms the PTM approach thanks to its linear complexity with the number of logic gates in the circuit. Nonetheless, the more reconvergent fanouts there are in the circuit, the more SPR loses accuracy in computing the circuit reliability. The SPR-Multi Pass (SPR-MP) method has been then proposed to enhance the original SPR algorithm by tackling the problem of reconvergent fanouts [13]. Indeed, SPR-MP takes into account the correlation of signals by performing the analysis in multiple passes. A single state of the fanout signal is considered in each pass. Thus, there are 4 possible passes for each fanout, corresponding to four partial reliability values that should be added in the end. Like the PTM approach, the SPR-MP is an accurate algorithm. However, its complexity grows exponentially with the number of reconvergent fanouts in the circuit. It is worth mentioning that all PTM, SPR and SPR-MP methods are originally developed to evaluate the vulnerability of combinational circuits to transient faults. However, they do not consider the realistic glitch modeling of such faults. They assume a transient error lasts for a whole cycle. That is why, the SPR-MP could also be applied to model permanent faults. This can be done by substituting the reliability of the gate 'q' for the complementary of the detection probability (1-FR). And as we deal with a single defect model, all 'q' are set to 1, except that of the faulty gate.

III. Proposed Methodology for Defect Tolerance Analysis

Exhaustive analog fault simulations are impossible due to the intractable simulation time and to the huge memory needed. On the other hand, accurate results of defect tolerance can not be generated at a gate level analysis since it limits defect types to the ones affecting nets between logic gates in the circuit. Hence, models developed at the gate level for defect tolerance estimation should take into account the intrinsic fault contribution of the logic gates. Here, we propose a methodology that mixes transistor and gate level analyses in order to accurately estimate the defect tolerance of combinational circuits. In this section, we describe the proposed method developed as an analytical model, and implemented by means of fault-simulation and fault-injection techniques. We present the defect tolerance design flow integrated as a part of the classical one.

A. Mixed transistor-gate defect tolerance analysis

Let G=($g_1, g_2, ..., g_n$) be an implementation of a given combinational circuit synthesized in a standard cell library. Let $FR(g_i)$ be the detection probability corresponding to the probability that the circuit fail when the defect takes place in gate g_i. As we deal with a single defect model, the global detection probability of the circuit is expressed in (1) where n is the number of the gates constituting the circuit.

$$F = \frac{1}{n} \sum_{i=1}^{n} FR(g_i) \tag{1}$$

Here, $FR(g_i)$ corresponds to the probability that at least one of the circuit outputs is incorrect due to a transistor-level defect affecting the gate. This means, first that the defect affected the output of the gate itself and second that this fault reached the output of the circuit without being logically masked. These two phases are totally independent and could be classified into transistor and gate-level propagations. Therefore, the detection probability $FR(g_i)$ can certainly be written as the product of the detection probabilities due to transistor and gate level propagations.

Transistor-level propagation results in altering the gate output because of a defect occurring within the gate. Let us define FR^i the probability that the output of the gate g_i fails due to an inner defect. Two cases are to be considered: either the fault-free output value is a logic '0' and the obtained output is at logic '1' or the correct output value is '1' and the output is inverted. We define (FR^i_{01}, FR^i_{10}) the probabilities that the output of the gate g_i is incorrect and the error is a ('0'→'1', '1'→'0') inversion. We will describe later on how to extract these parameters from a transistor-level fault analysis using the CellModelGen tool.

At gate level, the defect can be modeled by the stuck-at fault model, where a net is stuck at the logical value '0' or '1'. Using fault injection methods or analytical methods such as Binary Decision Diagrams (BDD) representation, the probabilities that the stuck-at error affects the circuit outputs can be calculated. Let us define (FR^i_{st0}, FR^i_{st1}) as the probabilities that at least one of the outputs of the circuit is incorrect due to a (stuck-at-0, stuck-at-1) at the output of the gate g_i. The expressions of FR^i_{st0} and FR^i_{st1} can be calculated using (2), where $outBin$ and $outCorrBin$ correspond to logical values of the obtained and the correct output signals with the considered input sample j, respectively. N represents the number of relevant input combinations according to the considered fault. As a matter of fact, the interesting input combinations for a stuck-at-0 fault are those for which the

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node is supposed to be at logic value ‘1’. Likewise, the interesting input combinations for stuck-at-1 error are those for which the node is supposed to be at logic value ‘0’.

$$FR^i_{st} = \frac{1}{N}\sum_{j=1}^{N}(outBin(j) \oplus outCorrBin(j)) = \frac{1}{N}\sum_{j=1}^{N} F_{ij} \quad (2)$$

Taking into account the detection probabilities of the gate (FR^i_{01}, FR^i_{10}) and the propagation probabilities using the stuck-at model (FR^i_{st0}, FR^i_{st1}), the expression of the gate detection probability can be easily derived from (3).

$$FR(g_i) = FR^i_{01}FR^i_{st1} + FR^i_{10}FR^i_{st0} \quad (3)$$

Let us consider the example depicted in Fig. 1. The circuit is made up of 2 OR gates. Assume that ($FR^{OR}_{01}, FR^{OR}_{10}$) have been extracted from analog fault simulation. The output S_1 can be faulty due to a defect that takes place in g_1 or in g_2. As g_1 and g_2 can not be defective at the same time, and considering that the defect has the same probability to occur in either cell, the global detection probability of the circuit will be $F = \frac{1}{2}(FR(g_1) + FR(g_2))$. Now, suppose that H exhibits a ‘0’→‘1’ fault inversion, due to a defect occurring in g_1. From the truth table of the circuit shown in Fig. 1, this can happen only for the first two stimuli, where H is normally at logic value ‘0’. $H^{(f)}$ denotes the faulty value which corresponds to $\bar{H}$, as the fault has occured in node H. $S_1^{(f)}$ is the value of the output when H is faulty. We can see that the output S_1 is affected just once. In this case, the number of relevant stimuli N and the $\sum_{j=1}^{N} F_{ij}$ shown in (2) are equal to 2 and 1, respectively. Therefore, $FR^1_{st1} = \frac{1}{2}$. The same reasoning is applied when H fails with a ‘1’→‘0’ inversion. In that case, $N = 6$ and the number of times that the failure propagates to the output equals 3. Hence, $FR^1_{st0} = \frac{3}{6}$. Using (3) we can deduce $FR(g_1)$. $FR(g_2)$ could be likewise computed. However, since the circuit output S_1 is itself the output of g_2, one can deduce directly that $FR(g_2)$ is simply the detection probability of the OR gate which is the sum of FR^{OR}_{01} and FR^{OR}_{10}.

We have simulated the circuit shown in Fig. 1, using a 65nm industrial CMOS technology and considering just stuck-open and stuck-closed transistor defects, as they are the most common ones [17]. Table I shows simulation results, compared to those obtained with our model.

Through analog fault simulation, the intrinsic detection probabilities of the OR gate (FR^{OR}_{01}, FR^{OR}_{10}), the failure contribution of the gates ($FR^{simu}_{g_1}$, $FR^{simu}_{g_2}$) and the total detection probability of the circuit F^{simu}_{total} were extracted. $FR(g_1)$, $FR(g_2)$ and F^{model}_{total} are calculated from the model previously detailed. We observe that the detection probability of g_1 is correctly computed by the proposed model, while the obtained detection probability of g_2 is 20% more than the exact value. This leads to 9.98% error on the total detection probability of the circuit as shown in the last column of Table I.

Actually, this model does not take into account the probabilities of the gate input combinations. It considers that the gate has a constant detection probability whatever its inputs are. Yet, the fault can be masked by some input combination and be detected by others. So, the only explanation of the obtained error is that there is a disproportionality in the number of detected defects per stimulus while the model considers the mean over all stimuli. To ameliorate this model, we propose to take into account the contribution of each input combination apart and their probabilities.

We define the conditional detection probabilities ($FR^i_{01/k}$, $FR^i_{10/k}$) as the probabilities that the output of the gate g_i is incorrect with a (‘0’→‘1’, ‘1’→‘0’) inversion, and given that the input combination of the gate equals k. For instance, for 2-input gates, 4 possible input combinations exist. Hence, 8 conditional detection probabilities characterize the gate: ([$FR_{01/00}$, $FR_{01/01}$, $FR_{01/10}$, $FR_{01/11}$],[$FR_{10/00}$, $FR_{10/01}$, $FR_{10/10}$, $FR_{10/11}$]). To get the gate detection probability, (3) can be rewritten as (4), where w is the number of gate inputs, $p(k)$ is the probability of the gate input combination k and ($FR^i_{st0/k}$, $FR^i_{st1/k}$) are the conditional stuck-at detection probabilities taking into account the considered stimulus k.

$$FR(g_i) = \sum_{k=1}^{2^w} p(k)(FR^i_{01/k} \times FR^i_{st1/k} + FR^i_{10/k} \times FR^i_{st0/k}) \quad (4)$$

As a matter of fact, ($FR^i_{st0/k}$, $FR^i_{st1/k}$) can be derived using (2). And as each input combination k is considered apart, the relevant stimuli of the circuit are those generating the input combination k at the gate inputs. Hence, N in (2) can be written as $p(k) \times 2^m$, where m is the number of primary inputs. Substituing (2) into (4), the term $p(k)$ will be simplified and we get:

$$\begin{aligned} FR(g_i) = \frac{1}{2^m}\sum_{k=1}^{2^w} & FR^i_{01/k} \sum_{j=1}^{p(k)2^m} F_{ij/(st1,k)} \\ & + FR^i_{10/k} \sum_{j=1}^{p(k)2^m} F_{ij/(st0,k)} \end{aligned} \quad (5)$$

The terms $\left(\sum_{j=1}^{p(k)2^m} F_{ij/(st1,k)}, \sum_{j=1}^{p(k)2^m} F_{ij/(st0,k)}\right)$ are none other than the numbers of detected defects at the circuit outputs due to a (stuck-at-1, stuck-at-0) error, looping over all input combinations of the circuit giving the stimuli k at the gate inputs.

We apply the improved model to calculate the detection probability of the gate g_2 underestimated by the first model. Through analog fault simulation, we easily get the conditional detection probabilities of the OR gate shown in Table II(a). The number of detected defects due to a stuck-at(1,0) error at the output of the gate g_2 is given in Table II(b). The detection probability of the gate (g_2) can then be calculated as in (6) which corresponds to the same value obtained by Spice simulation.

$$\begin{aligned} FR(g_2) = \frac{1}{8}(& FR_{01/00} \times 1 + FR_{10/01} \times 3 \\ & + FR_{10/10} \times 1 + FR_{10/11} \times 3) \end{aligned} \quad (6)$$

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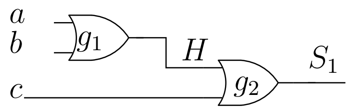

a	b	c	H	S_1	$H^{(f)}$	$S_1^{(f)}$
0	0	0	0	0	1	1
0	0	1	0	1	1	1
0	1	0	1	1	0	0
0	1	1	1	1	0	1
1	0	0	1	1	0	0
1	0	1	1	1	0	1
1	1	0	1	1	0	0
1	1	1	1	1	0	1

Fig. 1: Example of fault propagation.

TABLE I: Defect tolerance analysis of circuit in Fig. 1.

FR_{01}^{OR}	FR_{10}^{OR}	$FR_{g_1}^{simu}$	$FR_{g_2}^{simu}$	F_{total}^{simu}	$FR(g_1)$	$FR(g_2)$	F_{total}^{model}	$\epsilon(\%)$
0.125	0.125	0.125	0.2083	0.1666	0.125	0.25	0.1875	9.98

TABLE II: Conditional detection probabilities of OR gate (a) and number of detected defects due to a stuck-at(1,0) error at the output of the gate g_2 (b).

(a)

k	FR_{01}	FR_{10}
00	0.5	0
01	0	0.166
10	0	0.166
11	0	0.166

(b)

k	$st1$	$st0$
00	1	0
01	0	3
10	0	1
11	0	3

B. Transistor-level analysis : library characterization

With the Mentor Graphics Tessent CellModelGen tool, we could analyze the defect tolerance of each cell in the library. In this section, we describe the way the tool works and how we use it to extract the detection probabilities needed to perform accurate gate analysis thereafter.

The CellModelGen tool considers realistic locations of different types of defects (bridges, opens, T_{on}/T_{off}, port-opens and port-bridges). Actually, it uses the extracted netlist to create a list of potential defects originating from extracted capacitors, resistors, transistors and cell ports. Indeed, the extracted capacitors are candidates for bridge defects. Resistors are potential open defects. Transistors are candidates for stuck-closed (T_{on}) and stuck-open (T_{off}) defects. The ports could be port-open and port-bridge defects. In each simulation run, a single defect is injected in the original extracted netlist and analog fault simulation is performed for all possible input combinations. Then, the measured output is compared to the golden voltage corresponding to the output voltage of the fault-free netlist, to determine whether the defect was masked or not. For each defect and each stimulus, the detection information is reported in a so-called *defect matrix*. Equation 7 gives an example of a defect matrix where rows correspond to the input combinations (stimuli) and columns to the inserted defects. The letter 'D' in the position (i, j) means that the defect d_j is detected with the input combination i [10].

$$M = \begin{bmatrix} D & - & D & ... & - & - & - \\ - & - & D & ... & - & D & - \\ . & & & & & & \\ . & & & & & & \\ . & & & & & & \\ - & - & D & ... & - & - & - \\ D & D & - & ... & - & D & - \end{bmatrix} \quad (7)$$

As we deal with a single defect model, the detection probability (FR) of the gate is obtained by averaging the number of detected defects over the total number of tests. This is expressed in (8), where h is the total number of inserted defects and m is the number of inputs.

$$FR = \frac{1}{2^m}\frac{1}{h}\sum_{i=0}^{2^m}\sum_{j=1/M(i,j)=D}^{h} M(i,j) \quad (8)$$

The detection probabilities (FR_{01}, FR_{10}) defined in Section III-A are also extracted from the defect matrix by classifying the input combinations that result in logic value '0' or '1' at the fault-free output.

The conditional detection probabilities ($FR_{01/k}$, $FR_{10/k}$) are derived considering the single test where the input combination equals k. It can be written in (9) as the ratio between the number of detected defects in the k-th row over the total number of considered defects. Obviously, for each input combination k, one of the conditional detection probabilities $FR_{01/k}$ or $FR_{10/k}$ equals zero since the stimulus k in the input gate generates either the logic level '0' or '1' as correct output.

$$FR_{/k} = \frac{1}{h}\sum_{j=1}^{h} M(k,j) \quad (9)$$

This step should be included in a classical design flow, so as to perform a defect tolerance library characterization.

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C. Defect tolerance analysis methodology

Figure 2 shows the proposed methodology to evaluate the fault tolerance of combinational circuits. So, the first step is to perform a defect tolerance library characterization, which is a transistor-level analysis. The detection probabilities (FR_{01}, FR_{10}) and the conditional detection probabilities ($FR_{01/k}, FR_{10/k}$) are extracted for each library cell using the CellModelGen tool as previously described. Then, a database is created containing logic functions of the cells (NAND, NOR, ...) and their corresponding detection probabilities. Note that this step is done once per library. To our knowledge, this is the first attempt to extract realistic detection probabilities that can be used to feed a higher level model for more accurate result.

The second step is to do a gate-level analysis using a fault injection approach. For both proposed models, two different simulations with the fault-model stuck-at-0 then stuck-at-1 at the output are carried out, for each cell in the circuit. The number of times the obtained output is different from the fault-free output represents the failure coefficient F_{ij} shown in (2), and which serves to calculate the stuck-at detection probabilities. This step can be executed using a fault injection platform like the one proposed in [20].

The final step is to calculate the intrinsic contribution of defective elementary cells to the global detection probability of the circuit. Thus, an HDL parser identifies the logic function for each gate in the circuit so that the corresponding detection probabilities from the library database can be loaded. The name of the gate will be utilized to load its corresponding stuck-at detection probabilities generated in the second step. Then, detection probability of each elementary cell can be deduced using (3) (first model) or (5) (second model).

The global detection probability of the circuit is inferred from the expression in (1).

Note that this process is easily integrated in a classical design flow. Moreover, unlike the CellModelGen simulation needing the circuit layout to get the extracted Spice netlist, this method avoids tedious steps in the design flow. Indeed, the HDL description of the circuit along with a database characterizing the library defect tolerance allow to calculate the global detection probability of the circuit in an accurate manner, as will be proven in the next section.

IV. Experimental setup and simulation results

In this work, we have used the 65nm industrial CMOS process from STM. The intrinsic detection probabilities (FR_{01}, FR_{10}) and the conditional ones ($FR_{01/k}, FR_{10/k}$) are extracted for each library cell using the CellModelGen tool, as previously described. Then, a database is created containing the name of the cell and its corresponding detection probabilities. Table III shows an overview of the failure database containing some basic cells from STM library, and considering just stuck-open and stuck-closed transistor defects.

To get the stuck-at detection probabilities, we have used the platform proposed in [20]. This platform was implemented on FPGA and was designed as a hardware IP to accelerate the Fault Injection and Fault Masking Analysis (FIFA). For our study, for each gate in the circuit, we inject a stuck-at-0 and then a stuck-at-1 fault at its output to report the detection probabilities. For instance, Table IV shows the conditional stuck-at detection probabilities of the ISCAS85 c17 benchmark circuit shown in Fig. 3.

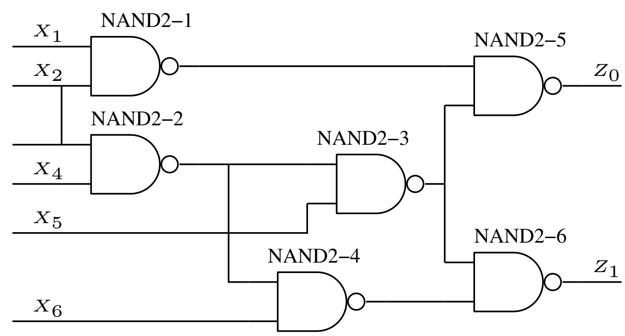

Fig. 3: c17 ISCAS85 benchmark circuit.

TABLE IV: The conditional stuck-at detection probabilities of c17 ISCAS85 benchmark circuit.

cell	NAND2-1		NAND2-2		NAND2-3	
k	FR_{st1}	FR_{st0}	FR_{st1}	FR_{st0}	FR_{st1}	FR_{st0}
00	0	4	0	6	0	4
01	0	6	0	6	0	4
10	0	4	0	6	0	11
11	6	0	6	0	11	0

cell	NAND2-4		NAND2-5		NAND2-6	
k	FR_{st1}	FR_{st0}	FR_{st1}	FR_{st0}	FR_{st1}	FR_{st0}
00	0	4	0	2	0	6
01	0	4	0	6	0	6
10	0	6	0	10	0	6
11	6	0	14	0	14	0

The proposed models are implemented to automatically calculate the detection probability of the circuit using the detection probabilities of its elementary gates and their correponding stuck-at detection probabilities. Table V reports the global detection probabilities and the individual detection probability of each cell in the considered c17 benchmark circuits. The third column corresponds to the value extracted using analog fault simulation by CellModelGen tool, which represents obviously the accurate one and will be used here as the reference. The fourth and the fifth columns represent the proposed models, where the second model is the improved one taking into account input combination probabilities. The last two columns are detection probabilities derived from SPR and SPR-MP approaches fed by realistic data obtained through transistor level library characterization. ϵ represents the relative error of the corresponding approach, compared to the reference CellModelGen simulation. The signs '$-$'/'$+$' mean that the models under/overestimate the fault tolerance value with respect to the reference one.

We notice that, like the SPR-MP, the proposed model taking

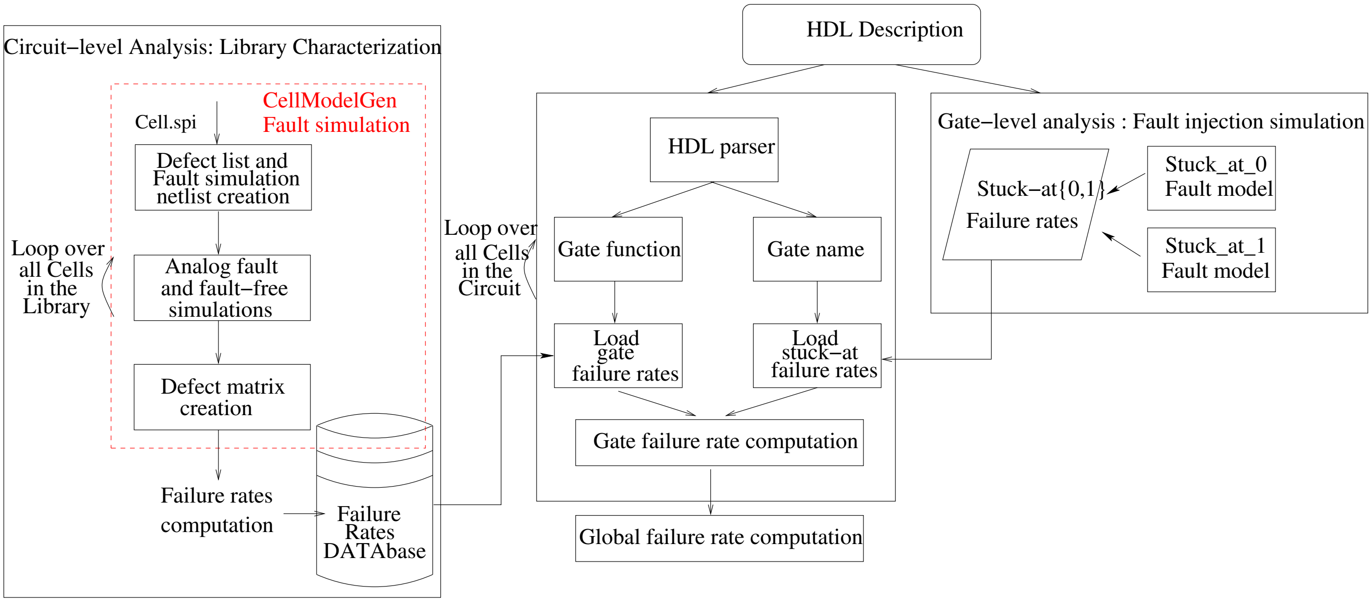

Fig. 2: Transistor/Gate defect tolerance design flow.

TABLE III: Failure characterization of 65nm STM library.

(a) Intrinsic detection probabilities

Logic Function	FR_{01}	FR_{10}	FR
AND2X4	0.2081	0.125	0.333
NOR2X3	0.125	0.125	0.25
NAND2X2	0.125	0.125	0.25
XOR2X18	0.142	0.1247	0.2667

(b) Conditional detection probabilities

Logic function	AND2X4		NOR2X3		NAND2X2		XOR2X18	
k	FR_{01}	FR_{10}	FR_{01}	FR_{10}	FR_{01}	FR_{10}	FR_{01}	FR_{10}
00	0.166	0	0	0.5	0	0	0.214	0
01	0.333	0	0.25	0	0	0.25	0	0.285
10	0.333	0	0.25	0	0	0.25	0	0.214
11	0	0.5	0	0	0.5	0	0.3571	0

TABLE V: c17 defect tolerance analysis.

		Ref	1^{st} model	2^{nd} model	SPR	SPR-MP
Circuit	Gate	FR	$\epsilon(\%)$	$\epsilon(\%)$	$\epsilon(\%)$	$\epsilon(\%)$
c17	NAND2-1	0.1718	- 3.02	0.00	- 9.08	0.00
	NAND2-2	0.1875	0.00	0.00	+ 21.76	0.00
	NAND2-3	0.2990	- 22.07	0.00	+ 28.39	0.00
	NAND2-4	0.1718	- 12.69	0.00	+ 13.68	0.00
	NAND2-5	0.3437	- 27.26	0.00	0.00	0.00
	NAND2-6	0.3125	- 20.00	0.00	0.00	0.00
	Global	0.2473	- 16.60	0.00	- 35.05	0.00

into account the input probabilities gives the exact value of the detection probability. Also, as expected when the cells have no reconvergent fanout, which is the case of (NAND2-5, NAND2-6) cells, the SPR gives an accurate result.

As a matter of fact, we simulated two other benchmark circuits: a 4-bit Ripple Carry Adder having 20 gates and 9 reconvergent fanouts, and also a 4-bit multiplier having 85 gates and 33 reconvergent fanouts. These two benchmarks could not be simulated using CellModelGen tool. Results obtained with our model confirm once again that we have the same accuracy as the SPR-MP method.

Furthermore, we simulated some ISCAS85 benchmark circuits considering 100.000 random input combinations. The results using the SPR-MP approach can not be generated at all for any considered circuit. Table VI shows the time needed

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to get the results using the proposed method. Here, the gate level analysis is performed using an FPGA with a frequency of 100MHz.

TABLE VI: Runtimes for ISCAS85 benchmark circuits.

Circuit	# of Gates	# of I/Ps	# of O/Ps	# of fanouts	Time (min)
c432	160	36	7	89	0.6
c499	202	41	32	59	0.8
c1355	546	41	32	259	2.1
c1908	880	33	25	385	3.5
c3540	1669	50	22	579	6.6
c6288	2416	32	32	1456	9.6

V. Conclusion

In a context where reliability evaluation has become a crucial fact in the design of digital circuits, we propose an efficient methodology to accurately assess the defect tolerance of combinational circuits. This methododology is implemented as a simple tool, easily integrated in a classical design flow. For different benchmark circuits, the proposed approach proved to be as accurate as two reference methods used for reliability assessment (CellModelGen tool and SPR-MP). As a matter of fact, our approach used the accurate transistor detection probabilities to deduce those at gate level. It also may be projected to higher levels. For instance, block detection probabilities could be computed from gate ones. Indeed, in our current study, we dealt with the single defect model. Therefore, as a future work, we plan to adjust the proposed method to the case of multiple defects affecting the circuit.

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Magnus effect in the fluid-film bearings

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***Abstract*—**One of the most important stages of mathematical modeling of the complex physical processes is to highlight the significant and to omit insignificant elements of the model. The goal of this paper is to detect and to justify the basic parameters and operational conditions of the fluid-film bearings where the Magnus effect cannot be neglected. A Navier-Stokes equation is used a mathematical model, considering the non-stationarity of the process, influence of the inertia forces, viscous resistance and mass forces and the condition of incompressibility of the continuous media. As a result of the analysis the conditions were determined, where the inertia forces from the Magnus effect significantly exceed the viscosity forces and the mass forces; considering these conditions the analytical form was obtained to determine the hydrodynamic reaction of the fluid film.

***Keywords*—**Continuum mechanics, hydrodynamic lubrication theory, Magnus effect, fluid-film bearing, similarity criterion.

I. Introduction

The Magnus effect [1] occurs with the combination of the rotational flow and the oncoming flow of the media around the body, which results in the drop of the pressure and in the resulting force perpendicular to the direction of the oncoming flow.

According to the Joukovsky theory on the lifting force [2] the Magnus effect in the quantitative terms is as follows:

$$\vec{F} = -\rho\vec{\Gamma}\times\vec{V}_{\infty}\,, \qquad (1)$$

where ρ - density of the media, $\vec{\Gamma}$ - circulation of the rotational velocity of the cylinder, $\vec{V}_{\infty}$ - velocity of the oncoming flow.

The module of the reaction (1) in the case of the flow over the cylinder of the unit length can be written in a more simple form suggested by Rayleigh [3]:

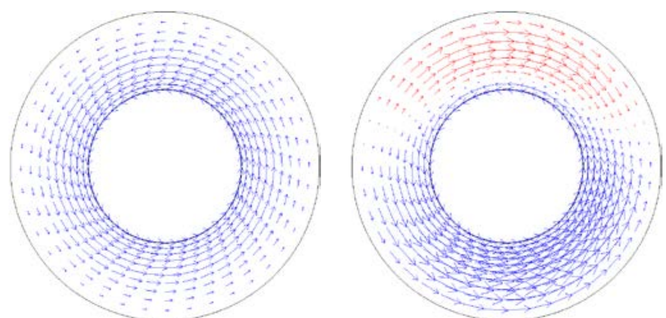
$$F = 2\pi\omega r^2\rho V_{\infty}\,, \qquad (2)$$

where ω - the angular rotational velocity of the cylinder, r - radius of the cylinder.

The Magnus effect in connected with the viscosity properties of the media, namely the stratified flow and adhesion properties, and quantitatively it is due to the inertia forces of the media motion, which is evidenced by the presence of the ρ in (1).

The object of the study is a circular flow of the viscous incompressible media in the fluid-film bearings. The importance of the correct calculation is hard to overestimate. It is only necessary to highlight that they are the key elements of the rotor systems in the fluid rocket engines.

The vibration of the rotating tip in the fluid-film bearing cause the media motion (fig. 1) in the same way as it happens when the oncoming flow flows over the rotating cylinder. So there is a theoretical possibility of a significance of the influence of the Magnus effect on the hydrodynamic reaction of the lubricant.



a b

Fig. 1 Vector field of the media flow in the bearing with the rotation tip, the center of which is stationary (a) or vibrates in the horizontal directions (b)

It is possible to show that the Reynolds equation [4] which is most frequently used in hydrodynamic theory, does not consider the influence of the Magnus effect. So it is an urgent problem to indicate the conditions of occuring and to evaluate the significance of the Magnus effect in the fluid-film bearings, as it is the objection of this paper.

II. Conceptual model

A problem under study considers a media flow in the gap between the tip of the rotor with the radius r which rotates and

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vibrates, and the bearing with the radius R of the rotor machine (fig. 2).

Some of the assumptions in the conceptual model are made subjectively, due to the fact of solving some particular class of problems of the hydrodynamics [5]. Among them are the following:

1. The rotor rotates with a constant angular velocity ω and vibrates in the plain which is perpendicular to its axis.
2. The continuous media is incompressible and has constant mechanical and thermophysical properties.
3. On the surfaces of the tip and the bearing the no-slip condition is met.

Another part of the assumptions was made on the basis of the results of the experimental study on the bearing dynamics of the high-speed lightly loaded rotor systems [6].

4. The media motion occurs in the plain perpendicular to the bearing axis, the lubricant consumes the whole area between the tip and the bearing.
5. The axis of the tip vibrates close to the center of the bearing.
6. The transverse vibrations frequency in equal to the rotational frequency, and the trajectory of the vibration is close to a circle form.

A third part of the assumptions will be formed based on the similarity theory and the dimensional analysis applied to the equations of the mathematical model of the media flow.

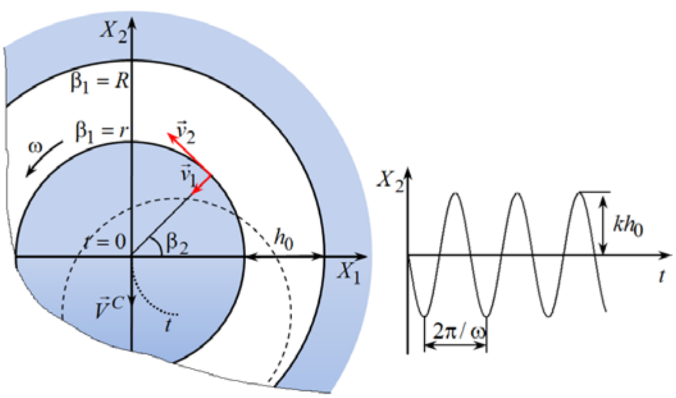

Fig. 2 Conformity model of the fluid-film bearing

III. The Mathematical Model

According to the assumptions of the conceptual model, and taking for the sake of simplicity that the trajectory of the vibrations of the tips is a circle of a known radius kh_0 ($0 \le k < 1$) with a center on a horizontal symmetry axis of the bearing and goes at initial point of time $t = 0$ through the center of the bearing (fig. 2), so the problem of the continuous media motion at this point of time is significantly simplified due to the symmetry of the flow area and the convenience of setting the boundary conditions. Below the problem of the continuous media flow in the gap between the tip of the rotor and the bearing, given their coaxial position, will be considered with vibrational and rotational rotor motion. To obtain the approximate analytical dependencies for the lifting force calculation, the analysis of the significance of the mathematical model equation terms will be implemented on the surface of the tip at an initial point of time.

The continuous media motion is more convenient to study in polar coordinates [7]. Lamé parameters h_i in polar coordinates β_i, where β_1 - a radial coordinate, β_2 - a tangential coordinate, will take the following form:

$$\begin{aligned} h_1 &= 1, \\ h_2 &= \beta_1. \end{aligned} \tag{3}$$

The Navier-Stokes equation in the projection on the β_i axis considering (3) take the following form [5], [8], [9]:

$$\begin{aligned}
&\rho\left\{\frac{\partial v_1}{\partial t} + v_1\frac{\partial v_1}{\partial \beta_1} + \frac{v_2}{\beta_1}\frac{\partial v_1}{\partial \beta_2} - \frac{v_2^2}{\beta_1}\right\} = \rho f_1 - \\
&-\frac{\partial p_0}{\partial \beta_1} + \frac{\mu}{\beta_1^2}\left[\beta_1^2\frac{\partial^2 v_1}{\partial \beta_1^2} + \beta_1\frac{\partial v_1}{\partial \beta_1} - v_1 + \frac{\partial^2 v_1}{\partial \beta_2^2} - 2\frac{\partial v_2}{\partial \beta_2}\right], \\
&\rho\left\{\frac{\partial v_2}{\partial t} + v_1\frac{\partial v_2}{\partial \beta_1} + \frac{v_2}{\beta_1}\frac{\partial v_2}{\partial \beta_2} + \frac{v_1 v_2}{\beta_1}\right\} = \rho f_2 - \\
&-\frac{1}{\beta_1}\frac{\partial p_0}{\partial \beta_2} + \frac{\mu}{\beta_1^2}\left[\beta_1^2\frac{\partial^2 v_2}{\partial \beta_1^2} + \beta_1\frac{\partial v_2}{\partial \beta_1} - v_2 + \frac{\partial^2 v_2}{\partial \beta_2^2} + 2\frac{\partial v_1}{\partial \beta_2}\right],
\end{aligned} \tag{4}$$

where v_i - components of the velocity vector of the media flow in the polar coordinates β_i, t - time, f_i - specific mass force, p_0 - pressure, μ - dynamic viscosity coefficient (viscosity).

The left hand part of the equations (4) characterize the inertia forces, the first term of the right hand part characterizes the mass forces (gravity, electromagnetic interaction forces), the second term of the right hand part is a hydrostatic force, the third term is a viscosity forces (dissipative term).

The incompressibility condition takes the form [5, 8, 9]:

$$\frac{\partial v_1}{\partial \beta_1} + \frac{1}{\beta_1}\frac{\partial v_2}{\partial \beta_2} + \frac{v_1}{\beta_1} = 0. \tag{5}$$

The equations of the vibration of the center of the tip in the X_i coordinates with the given assumptions take the following form[1]:

$$\begin{aligned} X_1^C &= -kh_0 \cos\omega t + kh_0, \\ X_2^C &= -kh_0 \sin\omega t, \end{aligned} \tag{6}$$

where k - amplitude of the vibration coefficient ($0 \le k < 1$),

[1] The values in the Cartesian coordinates are denoted with the capital letters (X, V, F, etc.)

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h_0 - average gap ($h_0 = R - r$), ω - rotational velocity of the vibrations (coincides the angular velocity of the rotor).

Obviously, the components of the velocity of the tip center in the X_i coordinates take the form:

$$\begin{aligned} V_1^C &= kh_0\omega \sin \omega t, \\ V_2^C &= -kh_0\omega \cos \omega t. \end{aligned} \tag{7}$$

Then, at the point of time $t = 0$ the cinematic boundary conditions take the form:

$$\begin{aligned} v_1\big|_{\beta_1 = r} &= V_1^C\Big|_{t=0} \cos\beta_2 + V_2^C\Big|_{t=0} \sin\beta_2, \, v_1\big|_{\beta_1 = R} = 0, \\ v_2\big|_{\beta_1 = r} &= \omega r + V_1^C\Big|_{t=0} \sin\beta_2 + V_2^C\Big|_{t=0} \cos\beta_2, \, v_2\big|_{\beta_1 = R} = 0. \end{aligned} \tag{8}$$

It can be shown that on the surface of the tip $\beta_1 = r$ the incompressibility condition (5) with the cinematic boundary conditions (8) take the form:

$$\frac{\partial v_1}{\partial \beta_1} = 0\,. \tag{9}$$

Additionally, with the (7) and (8) on the surface of the tip $\beta_1 = r$ the form of the functions $\partial v_i / \partial\beta_2$ and $\partial v_i / \partial t$ can be simply determined.

Then a similarity theory and a dimensional analysis are applied to evaluate the significance of the terms in the Navier-Stokes equation (4) and the incompressibility condition (5) in order to simplify the mathematical model (table I).

I The components of the Navier-Stokes equations (4) and the continuity equation (5)

Dimensional form		Dimensionless form
Value	Range	
Radial coordinate	$r \le \beta_1 \le R$	$\tilde{\beta}_1 = (\beta_1 - r)/h_0$
Tangential coordinate	$0 \le \beta_2 \le 2\pi$	$\tilde{\beta}_2 = \beta_2 / 2\pi$
Time	$0 \le t \le \infty$	$\tilde{t} = \omega t$
Radial component of velocity	$-kh_0\omega \le v_1 \le$ $\le kh_0\omega$	$\tilde{v}_1 = \dfrac{v_1}{2kh_0\omega}$
Tangential component of velocity	$\omega r - kh_0\omega \le v_2 \le$ $\le \omega r + kh_0\omega$	$\tilde{v}_2 = v_2 / v^*$, $v^* = \sqrt{(\omega r)^2 + (2kh_0\omega)^2}$
Mass force	$-g \le f_i \le g$	$\tilde{f}_i = f_i / g$
Pressure	$p_0 \sim p_0^0$	$\tilde{p}_0 = p_0 / p_0^0$

Due to the fact that to determine the lifting force it is necessary to solve the Navier-Stokes equation on the surface of the tip $\beta_1 = r$, the nondimensionalization of the equations of the mathematical model was implemented with the a priori knowledge of the range of the equation terms change on the surface of the tip.

The Navier-Stokes equations (4), written in a dimensionless form (table I) on the surface of the tip $\beta_1 = r$ take the form:

$$\begin{aligned} &\left\{ \frac{2k(h_0\omega)^2}{v^{*2}} \frac{\partial \tilde{v}_1}{\partial \tilde{t}} + \frac{2k(h_0\omega)}{(\tilde{\beta}_1 + \gamma)v^*} \tilde{v}_2 \frac{\partial \tilde{v}_1}{\partial \tilde{\beta}_2} - \frac{\tilde{v}_2^{\,2}}{(\tilde{\beta}_1 + \gamma)} \right\} = \\ &= \frac{\tilde{f}_1}{Fr} - Eu \frac{\partial \tilde{p}_0}{\partial \tilde{\beta}_1} + \frac{2k(h_0\omega)}{Re(\tilde{\beta}_1 + \gamma)^2 v^*} \left[-\tilde{v}_1 + \frac{\partial^2 \tilde{v}_1}{\partial \tilde{\beta}_2^2} - \frac{\partial \tilde{v}_2}{\partial \tilde{\beta}_2} \right], \\ &Sh\left\{ \frac{2k(h_0\omega)}{v^*} \frac{\partial \tilde{v}_2}{\partial \tilde{t}} + 2k\tilde{v}_1 \frac{\partial \tilde{v}_2}{\partial \tilde{\beta}_1} + \frac{2k\tilde{v}_2}{(\tilde{\beta}_1 + \gamma)} \frac{\partial \tilde{v}_2}{\partial \tilde{\beta}_2} + \frac{2k\tilde{v}_1\tilde{v}_2}{(\tilde{\beta}_1 + \gamma)} \right\} = \\ &= \frac{\tilde{f}_2}{Fr} - \frac{Eu}{2\pi(\tilde{\beta}_1 + \gamma)} \frac{\partial \tilde{p}_0}{\partial \tilde{\beta}_2} + \frac{1}{Re(\tilde{\beta}_1 + \gamma)^2} \left[(\tilde{\beta}_1 + \gamma)^2 \frac{\partial^2 \tilde{v}_2}{\partial \tilde{\beta}_1^2} + \right. \\ &\left. + (\tilde{\beta}_1 + \gamma) \frac{\partial \tilde{v}_2}{\partial \tilde{\beta}_1} - \tilde{v}_2 + \frac{2k(h_0\omega)}{v^*} \left(\frac{\partial^2 \tilde{v}_2}{\partial \tilde{\beta}_2^2} + 2 \frac{\partial \tilde{v}_1}{\partial \tilde{\beta}_2} \right) \right], \end{aligned} \tag{10}$$

where k - dimensionless coefficient of the vibrations amplitude ($k \le 1$), $v^* = \sqrt{(\omega r)^2 + (2kh_0\omega)^2}$ - characteristic velocity, $\gamma = r/h_0$ - geometry parameter, $Fr = v^{*2}/(gh_0)$ - Froude number, $Eu = p_0^0 / (v^{*2}\rho)$ - Euler number, $Re = v^* \rho h_0 / \mu$ - Reynolds number, $Sh = h_0 / (t_0 \omega r)$ - Strouhal number.

In many cases the substitution of the specific values of the dimensionless criteria in the dimensionless equations of the mathematical model allows to eliminate the non-significant terms of the model and simplify the model. Below these examples will be shown.

IV. Hydrodynamic force from the Magnus effect in the fluid-film bearings

On the basis of the developed mathematical model with the initial and boundary conditions it is necessary to determine, under which circumstances the influence of the Magnus effect on the resulting hydrodynamic force is significant. For this, the problem of determination of the horizontal component R_1 of the hydrodynamic reaction $\vec{R}$, which acts on the rotating cylinder of a unit length, is considered. The reaction is determined in the Cartesian coordinates X_i (fig. 2), nonzero value of this reaction evidences the presence of the Magnus effect.

To solve this it is sufficient to determine the function of the pressure distribution on the surface of the rotating cylinder from the second equation (4) considering the incompressibility condition (5), and then to determine an integral of the following form:

$$F_1 = -r \int_0^{2\pi} p_0 \big|_{\beta_1 = r} \cos\beta_2 d\beta_2 . \qquad (11)$$

Let us consider a particular case, where the mathematical model parameters have the values of such orders which are close to the conditions of the high-speed rotor systems fluid-film bearings operation. For such systems $\gamma \sim 10^2$ or less, so in the characteristic velocity equation $v^* = \sqrt{(\omega r)^2 + (2kh_0\omega)^2}$ the peripheral speed is no less than 10^2 times more than the vibration velocity, since $r = \gamma h_0$ and $k < 1$. Then the characteristic velocity is approximately equal to the peripheral velocity on the surface of the tip $v^* \approx (\omega r)$. The order of the terms in (9) for the case in question is shown in the table II.

II The Navier-Stokes equation (9) terms orders of magnitude

Inertial, $\times Sh$				Mass	Pressure gradient	Dissipative, $\times$Re				
$\frac{k}{\gamma^2}$	0	$\frac{k}{\gamma^2}$	$\frac{1}{\gamma}$	$\frac{1}{Fr}$	Eu	0	0	$\frac{1}{\gamma^3}$	$\frac{1}{\gamma^3}$	$\frac{1}{\gamma^3}$
$\frac{k}{\gamma}$	k	$\frac{k}{\gamma}$	$\frac{k}{\gamma}$	$\frac{1}{Fr}$	$\frac{Eu}{\gamma}$	1	$\frac{1}{\gamma}$	$\frac{1}{\gamma^2}$	$\frac{k}{\gamma}$	$\frac{k}{\gamma}$

The terms of inertia and dissipation can be neglected as their order differs by two or more orders from the order of the older terms. The same principle is applied to determine the conditions when the mass and dissipative terms can be totally neglected: $kSh \geq \max(1/Fr, 1/\mathrm{Re})$, or in the form of the rotational speed $\omega \geq 10 \max\left(\sqrt{g/(kr)}, 10\mu/(k\rho h_0^2)\right)$. Then the Navier-Stokes equations (4) take the following simplified form:

$$\rho \frac{v_2^2}{\beta_1} = \frac{\partial p_0}{\partial \beta_1},$$
$$-\beta_1 \rho v_1 \frac{\partial v_2}{\partial \beta_1} = \frac{\partial p_0}{\partial \beta_2}. \qquad (12)$$

If one differentiates the first equation (12) with respect to β_2, and the second – to β_2, and then subtract one from another and analyze the order of the terms, the constancy of the velocity gradient component $\partial v_2 / \partial \beta_1 = \omega r / h_0$ can be proven. Then, it is possible to determine the pressure distribution on the surface of the tip $\beta_1 = r$ from the equation (12) considering the boundary conditions (8) with precision up to the constant p_0^0:

$$p_0 = p_0^0 - k\rho r^2 \omega^2 \cos\beta_2 . \qquad (13)$$

Then, it is possible to determine the force which characterizes the Magnus effect in the fluid-film bearing:

$$F_1 = \pi k h_0 \omega^2 r^3 \rho = \pi\gamma\omega r^2 \rho V^C , \qquad (14)$$

where $V^C = kh_0\omega$ - amplitude of the velocity of the tip vibration (7).

The obtained equation with precision up to $\gamma / 2$ matches the initial calculation equation (2) obtained when solving the problem of the flow over the rotating cylinder by the oncoming flow. When the vibrations are not present $k = 0$, the mathematical model equations are reduced to the form for the case of the fluid flow between the rotating coaxial cylinders.

V. Conclusion

In the fundamental papers on the hydrodynamic lubrication theory [2], [3] the problems of stationary or quasi-stationary media flow are considered. And presently the majority of the articles in the field of the hydrodynamic lubrication theory and the rotor system dynamics are based on the Reynolds equation solution [10]-[12]. The reason for the present research is the fact that the media flow in the fluid-film bearing with a vibrating tip is close to the oncoming flow over the cylinder, so the Magnus effect from the inertial forces, not considered in the Reynold equation, can be significant.

At the present stage of the research the analysis of the dimensionless equations of the mathematical model of the non-stationary isothermal flow of the viscous incompressible media in the fluid-film bearing considering the mass forces, inertial forces and dissipation was made. The conditions were set, when the Magnus effect from the inertial forces action has the most significant effect on the hydrodynamic reaction of the fluid film. For such conditions, based on the approximate equations of the mathematical model, an analytical equation was obtained for the further calculation of the hydrodynamic force. So, the Magnus effect can affect significantly on the dynamics of the bearings and contactless sealing elements of the high-speed rotor machines when lubricated with the low-viscosity media, e.g. liquefied gas.

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On Modeling European Energy Exchanges as Small-World Phenomena

Leonarda Carnimeo, Michele Dassisti

***Abstract*—**In the last years, the European Commission adopted an energy policy for Europe with several documents including an action plan to meet the major energy challenges Europe has to face. A farsighted diversified yearly mix of energies was suggested to countries, aiming at increasing security of supply and efficiency, but a systemic view of energy exchanges between states is still missing. Energy import/export exchanges between European States suggest that economic/political relations between countries cause unpredictable behaviors for the European energy exchange network. This network is herein investigated from a modeling point of view. European annual exchanges of energy appear to present *Small World phenomena,* when supposing that connections between States are characterized by probability values depending on economic/political relations between countries.

***Keywords*—**Energy Export exchanges, Energy Import exchanges, European Energy Mix, Small World Phenomenon

I. Introduction

In the last years the European Commission stated that the implementation of an ambitious European energy strategy, covering all available energy sources, aims at beginning a new industrial revolution, with the objective of making EU more secure, competitive, sustainable and at a low energy consumption from an economic point of view [1]. In 2007, the European Commission adopted a precise energy policy for Europe [2] supported by several documents on various aspects of energy and including an action plan to meet the major energy challenges Europe has to face [3-6]. For this purpose, the adoption of a farsighted diversified yearly mix of energies was suggested to all Member States, aiming at increasing security of supply and efficiency. Unfortunately, a wide and systemic view of energy interchanges between states was not available. In [7] a graphical representation of energy import/export exchanges between European States was used to identify the existence of a European energy exchange network at one-glance. The same network is herein investigated from a modeling point of view as in [8, 9], by supposing that connections can exist between States with a probability depending also on economic/political relations between countries. By embedding national economical agreements and exchanges, the resulting network can depend on both social issues and technical ones. For this purpose, the hypothesis that the *small-world phenomenon* is not only a feature of social networks [8] is herein assumed and a proposal is performed to evaluate if the mixed nature of structural energy exchanges in Europe, can be modeled with the so-called *small-world network.* In this way, the composition of annual National Energy Mix [3-6] can be better understood by a comparison of energy import/export values for each country.

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II. European Energy Exchanges

In 2006 the European Commission invited Member States to choose properly their Energy Mix, namely, the diversification of national energy supply [1]. For this purpose, the different nature of energy exchanges between pairs of countries has to be taken simultaneously into account. In most cases energy trade may not be optimal. Thus, the Green Paper was an important step in the development of EU energy policy to achieve economic, social and environmental challenges by facing Europe in the energy sector: increasing dependence on imports, volatility in fuel prices, climate change, increased demand and barriers to domestic energy. The situation of energy exchanges for each country can be highlighted at one-glance to show if the national energy flow reveals sustainable and efficient every year more by using graphic tools as in [7]. A proper composition of Annual National Energy Mix [3-6] can be highlighted by an immediate comparison of energy import/export values for each country. For this purpose, an energy data analysis has to be firstly performed in order to collect annual electric energy import/export flows in every European Country. These data can be grouped with respect to country, year and type of imported sourced (crude oil, gas, electric energy…). After processing available data to make them effectively comparable, they have to be analyzed with the aim of identify which type of energy sources is the most frequent in internal European exchanges. The electric Energy import/export exchanges have to be analyzed with respect to all Countries of the European area. Data related to Electric

Energy imports by Country of origin and data related to Electric Energy exports by Country of destination have been derived from Eurostat Databases [5, 6] within the period 1996 - 2010.

III. Small World Phenomenon

The ultimate goal of this study of European energy exchanges is to understand and explain how the unpredictable structure of exchanges can affect the overall efficiency of electrical fruition within EU, i.e., to set different models and derive sound conclusions on the potential effects of ruling strategies. The methodology herein suggested to analyze this network is based on graph theory. The main hypothesis is that the energy flow from/toward a country is represented by an edge of a network, whose length is provided by the overall annual energy exchange. The network then consists of a number *n* of vertices and a number *k of* edges connected to each vertex, where vertices represent countries at a high level of abstraction. The structural properties of the network could be quantified by evaluating the Characteristic Path Length (*CPL*) evaluated as the geodesic distance (shortest path) d_{ij} from vertex *i* to vertex *j*:

$$CPL = \frac{1}{\frac{1}{2}\, n\,(n-1)} \sum_{i \geq j} d_{ij} \qquad (1)$$

Moreover, the *Closeness Centrality* (*CC*) is a variable which measures how many steps are required to access every vertex starting from a given one. Considering each vertex as the geographical center of a generic state at a higher level of abstraction, it can be supposed that the higher the distance with other states is, the stronger the commercial exchange. Thus, the higher the distance, to a certain extent, the stronger the connection between vertices should be. This appears just as the opposite of the small world phenomenon. Nevertheless, indicators still maintain their effectiveness and can be accordingly used to draw sound conclusions. Thus, the amount of energy exchange will be represented by the weight of the corresponding edges.

Furthermore, the variable *Diameter* of the network can be also considered, by evaluating the weighted length of the longest geodesic path between any two vertices weighted by the amount of exchanged energy. In this analysis this measure has not a physical meaning; rather it represents a measure of the entity of each exchange in an opposite sense: the higher is the network diameter, the stronger the exchanges amongst countries are.

It has to be noticed that in this kind of analysis, energy exchanges are typically point-to-point ones. Also temporary exchanges are possible, but they are not visible in the available statistical data. Due to the fact that these edges are connected in a network, the meaning of the variable *distance* d_{ij} can be interpreted as a sort of energy *fluidity*, that is, the easiness of exchanges within the EU Area.

Another important index necessary for the analysis is the *RECiprocity index (REC)* defined as the ratio of all possible connected couples of vertices which have a reciprocal behavior [9]. To a certain extent, the measure of REC turns to be an interesting indicator of the degree of interconnection of the network, since the higher the index value, the stronger the mutual relationships between countries.

An analogous measure is defined as the *transitivity* (the probability that adjacent vertices of the *i*-th vertex are connected), also called *Clustering Coefficient* CC_i:

$$CC_i = 3\, \frac{no.(triangles\_connected)\ [vertex\_i]}{no.(triangles\_centered)} \qquad (2)$$

and globally

$$CC = 1/n \sum_{i} CC_i \qquad (3)$$

At least, an interesting value that may help us to understand or predict the behaviour of these systems is the *Small World Coefficient*, (*SMW*) calculated as

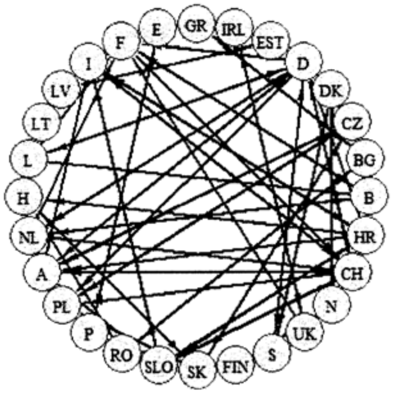
$$SMW = \frac{CPL}{CC} \qquad (4)$$

for a real network and taking as a reference the fully interconnected network (a completely oriented graph with *n*(*n*-1) edges) providing the information on edges sense: exiting/entering from/in a vertex in case of export/import, respectively.

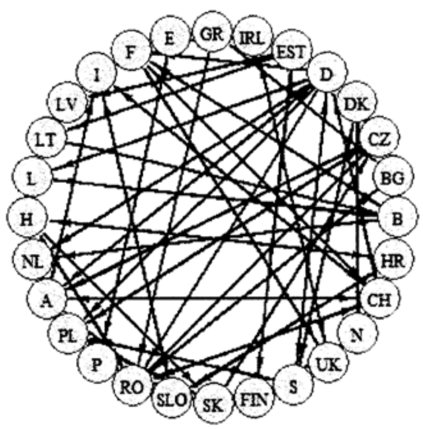
When analyzing the distribution of degrees of all vertices, it is interesting to draw an oriented graph of this small network. The *Degree* of vertices (DEG) can be adopted to analyze the graph, being the *degree of the i-th vertex* defined as the number of edges connected to that vertex: the maximum degree max-DEG can be an interesting synthesis indicator for a context analysis. Another interesting analysis to be performed is based on skewed degree distributions, i.e., the cumulative distribution of the number of vertices connected to any given one. This is an intriguing analysis to distinguish scale properties of the energy exchange network and to characterize it with respect to the small-world features too. The small-world effect could also be mathematically evident, if the number of vertices within a distance from a typical vertex grows exponentially with the distance [9]. After assessing import and export flows by country of origin and destination, the next step could eventually regard with the analysis of electric energy import/export flows between Countries in successive years.

IV. Model of the Energy Exchange Network

The whole European network, composed of 28 vertices, one for each country, has been modeled. This network is almost a virtual one, since its edges represent European energy exchange flows, even though these flows are subjected to the presence of physical connections. A comparative radial picture of the European network is provided at the extreme years of the period. In Fig.1 the network of energy exchanges is shown and it is almost stable in time, due to historical relationships between adjacent countries for political or social reasons. The same network, on the other hand, can be considered as unpredictable, since no general rule procedures for electrical exchanges appeared to be present at the time of analysis.



(a)



(b)

Fig.1 Radial representation of the European energy exchanges: (a) in 1997; (b) in 2010

Then, by observing the values of European variables in the next Table I and the values of CPL in the subsequent Fig.2, the idea that the network shows a small-world effect reveals justified.

Table I - Values of European variables in the Small World phenomenon

Year	CPL	CC	REC	Max-DEG	SMW
1997	2.768	0,447	0,725	19	3.816
2010	3.032	0,317	0,811	19	3.737

In the authors' opinion, the presence of small world phenomena can be further confirmed by means of a control charting scheme analysis that can be developed to construe again the small world indices adopted for the analysis of the full European energy exchange network.

V. Statistical perspective of the Small-world behaviour

Taking into account the Small World network composed by the whole European IEN as in [10], in the present paper, the previously drawn conclusions are even further discussed, by considering that the dynamical behavior of the network offered some interesting hints from a management point of view. Following the publicly available database of European electric energy exchanges, annual import/export flows are herein statistically analyzed for each European Country in the period 1996 – 2010. In particular, a statistical F test is performed to recognize the presence of the so called 'crisis effect', i.e., a change of behavior of two groups of data.

In this paper, the small world indices adopted for the analysis of the full European energy exchange network are re-interpreted according to a control charting scheme in order to explain better the time response of the network itself. This new point of view about the meaning of the indices will allow to assess the true dynamical perspective of the features of the small world network. The study reported in [10] draws main conclusions concerning with economic/political relations between countries by means of a sort of measure of 'sociality' and only those measures of 'sociality' are herein addressed.

In Fig. 2(a), where the CPL analysis is reported, the change in a given time around the year 2007-2008 can be noticed, confirming the variation observed in [10] in the same years.

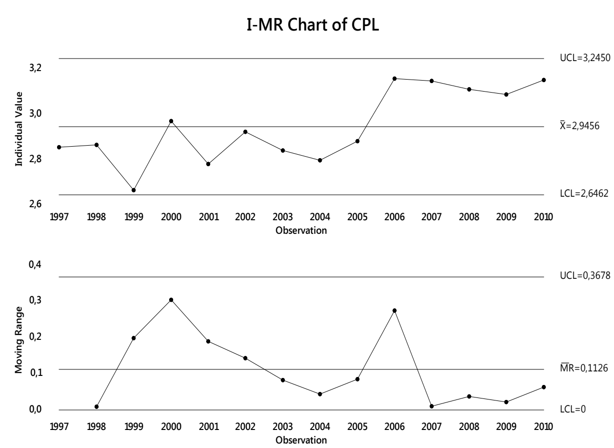


Fig. 2a. CPL Moving range control chart

The significant increase of CPL (and the corresponding decrease in variance) clearly indicates a variation in the network behaviour as well as the occurrence of a specific cause of CP increase. This fact can be indicated as an evidence of the 'sociality' feature of the energy network, provided that the electrical flows are related to human needs more than to technical requirements.

VI. Conclusions

In this work, the evolution of the European energy exchanges over the years 1996-2010 has been analyzed and modeled, highlighting some interesting behavioral features. In detail, European import/export energy exchanges have been investigated to verify if *Small World phenomena* are present in the whole European network by supposing that connections exist between States with probability values depending also on economic/political relations between countries. The evaluation of the defined indices from Eurostat data has indicated that the European network of energy exchanges appear to exhibit a Small-World behavior. Moreover, the Small-World features of the European energy exchange network have been analyzed by considering a control charting approach, which enables to appreciate the dynamical causes occurring to the system, thus detecting any anomalous behavior or degradation of the sociality of the network at a macro level. In detail, the significant increase of CPL and the corresponding decrease in variance have indicated an evidence of the 'sociality' feature of the energy network, provided that the electrical flows are related to human needs more than to technical requirements. This result was not highlighted in the previous work, since no hint of changes of the variance had been detected, but it has been obtained by means of the control charting scheme analysis herein performed. It has to be noticed that this feature reveals really promising from an energy management point of view, because it may offer new tools to design appropriately policy exchange rules, enabling to perform a sort of prediction of effects in European energy exchanges.

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Electric Vehicle Speed Control using Three Phase Inverter operated by DSP-based Vector Pulse Width Modulation Technique

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Abstract-Solar electric vehicles (SEV)are considered the future vehicles to solve the issues of air pollution, global warming, and the rapid decreases of the petroleum resources facing the current transportation technology. However, SEV are still having important technical obstacles to overcome. They includebatteriesenergy storage capacity, charging times, efficiency of the solar panels and electrical propulsion systems.Solving any of those problems and electric vehicles will compete - complement the internal combustion engines vehicles.In the present work, we proposean electrical propulsion system based on three phase induction motor in order to obtain the desired speed and torque with less power loss.Because of their lightweight nature, small volume,low cost less maintenance and high efficiency, a three phase squirrel cage induction motor (IM) is selectedfor the electrical propulsion system. The IM is fed from three phase inverter which is operated using constant V/F control method and Space Vector Pulse Width Modulation (SVPWM) algorithm. The proposed system uses Texas Instruments TM320F2812Digital Signal Processor (DSP) to generate SVPWM signal needed to trigger the gates of IGBT-based inverter.The experimental results show the ability of the proposed system to generate a three-phase sine wave signal with desired frequency. The system is also experimented on EVprototype which we manufactured and the results show that the EV prototype can be propelled to speed up to 60 km/h under different road conditions.

Key Words- Electric Vehicle, Squirrel Cage Induction Motor, SVPWM, V/F control, DSP processor, DMC library.

1 Introduction:

Efforts to improve air quality in heavily populated urban communities- by reducing vehicular emissions – have rekindled interest in the development of electric vehicle technology. However, the key issueswhich are challenging the design of electric vehicles are the electric propulsion system, energy sources and battery management system [1, 2]. Solving any of those issues and electric vehicles will compete - complement the conventional internal combustion engines vehicles.This paper will focus only on the electric propulsion system design.

DC and BLDC motor drives have been widely applied as propulsion system to EVs because of their technology maturity and control simplicity. However, with the emerging technology in switching semiconductors and digital signal processorsat reasonable costled to more interest in using AC induction motors instead of DC motor [3].
The AC induction motors especially the cage type,have lightweight, small volume, low cost, less maintenance, no commutation,high torque atlow speed and high efficiency. Theseadvantages are particularly important for EV applications.

As EVs propulsion, an AC induction motor drive is fed with a DC source (battery), which has approximately constant terminal voltage. Thus a variable frequency and variable voltage DC/AC inverter is needed to feed the induction motor[4]. The DC/AC inverter is constituted by power electronic switches and power diodes. The current generation of inverter is based on high speed power transistors, like IGBT and MOSFET.
Since the output of the inverter is a high frequency square wave, a high speed processor is needed to produce the proper switching sequence. Various switching techniques[5]are used

to generate PWM signal which is used to determine the amplitude and the frequency of the output voltage. Among the various PWM techniques, Space Vector Pulse Width Modulation (SVPWM) has advantages that made it the most switching techniques suitable for electric vehicles.The interesting features of this type of modulation is that it provides better DC-link utilization, more efficient use of DC supply voltage, produce less ripples and increase life time of drive[6]. It can be easily implementeddigitallyand hence offer the advantage to perform entire digital processing. The performance of SVPWM depends on the type of processor used for its implementation.Among the various processors available in the market, the most popular are the Texas Instrument DSP which holds about 70% of the market[8].TMS320F2xxx DSP series are high speed processors which havebeen developed by Texas Instrumentsespecially for industrial control applications, in particular for implementation of SVPWM algorithm to drive the switches of the inverter.

Since the vehicle speed can be monitored by the driver and desired speed can also be adjusted by the driver an open loop control with constant voltage/frequency (V/F) method is implemented to control the speed of the motor. The V/F is selected because it tries to achieve some features which are suitable for electric vehicles. These includewide speed span with constant motor torque, low starting current, acceleration and deceleration of the vehicle.
The objective of this study is to develop an electric propulsion system based on three phase squirrel cage induction motor, IGBT-based three phase inverter and advanced processor, such as DSP, implementing SVPWM algorithm for open loop speed control using V/F method of electric vehicle. The paper is organized as follows: first we discuss the SVPWM technique along with V/F method, second we discuss the mechanical part of the vehicle, and third we describe the electrical propulsion system and finally practical results obtained are presented along with conclusions.

2 Space Vector Pulse Width Modulation Techniques:

A number of Pulse width modulation (PWM) schemes are used to control the magnitude and frequency of AC output voltage of the inverter. The most widely used PWM schemes for three-phase voltage source inverters [7] are sine wave sinusoidal SPWM and space vector PWM (SVPWM).Since SVPWM is easily implement digitally, enable more efficient utilization of DC bus voltage, and generate sine wave with lower total harmonic distortion, it is most frequently preferable technique used in modern AC machines drives fed by inverters.The performance of an induction motor is improved when SVPWM technique is applied [6]. Details explanation of the SVPWM and SPWM techniques can be found in [7].Although SVPWM is more complicated than sinusoidal PWM, it is easily implemented using modern DSP based control systems. The SVPWM technique implemented into the existing TI Digital Motor Control (DMC) library reduces computation time and the number of transistor commutations[9, 10]. It therefore improves EMI behavior.

In this work, the constant voltage/frequency (V/F) method along SVPWM is used for open loop speed control of induction motor with a reasonable degree of accuracy.

3 V/F control method

The best way to vary the speed of the induction motor is by varying the supply frequency. It can be shown that the torque developed by the induction motor is directly proportional to the ratio of the applied voltage and the frequency of the supply[4]. By varying the voltage and frequency, but keeping their ratio constant, the torque developed can be kept constant throughout the speed range. In summary, using the V/F control method the following can be achieved: 1) the induction motor can be run typically from 5% of the synchronous speed up to the base speed (maximum vehicle speed), and the torque generated by the motor can be kept constant throughout this range; 2) the starting current is lower; 3) the acceleration and deceleration can be controlled by controlling the change of the supply frequency to the motor with respect to time.

4Design objectives:

The dimension and mechanical structure of the electric vehicle prototype manufactured and used in this study is shown in figure 2. The weight, volume and aerodynamic drag and rolling resistance effects have beencarefully considered in the design of the body of the vehicle [11].The design objectives are to attain maximum speed of 60 km/h with a total weight of 500 kg and acceleration time 0 to 60 km/h below 30 sec. Figure 1 is used to derive the desired driving power to ensure vehicle operation.

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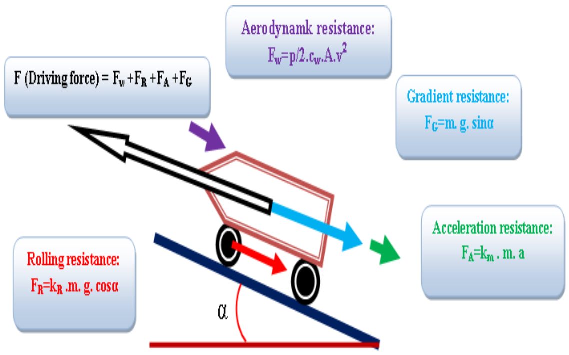

Figure 1: Representation of all forces acting on EV

The road slope torque T is defined by:

$$T_w = \frac{p}{2} \cdot c_w \cdot A \cdot \upsilon^2 \qquad (1)$$

$$T_R = k_R \cdot m \cdot g \cdot \cos\alpha \qquad (2)$$

$$T_A = k_m \cdot m \cdot a \qquad (3)$$

$$T_G = m \cdot g \cdot \sin\alpha \qquad (4)$$

$$T = T_w + T_R + T_A + T_G$$

Where; T_w is aerodynamic torque, T_R : rolling torque, T_A acceleration torque and T_G gradient torque.

Torque evaluation of the power flow occurring into a vehicle is in strong relation with its mass and a total couple will be expressed as:

$$C_t = T_A + T_p \qquad (5)$$

Where; m is a vehicle mass, C_t total torque, T_A acceleration torque, T_p permanent torque, α road angle.

For this study, we selected for the EVs propulsion a cage three phase induction motor of 4.7 kW 220/380 V 11/19 A with maximum speed of 1500 rpm. The solar panel station to refuel the vehicle batteries are shown in figure3.

Figure 2: Photo of the vehicle manufactured

Figure 3: Photo of the solar charging unit

5 Description of the Electrical Propulsion System

Figure 4 shows the block diagram of the open loop control system used to adjust the speed of the vehicle. The hardware includes squirrel cage induction motor, bridge inverter, isolation card, Digital Signal Processor (DSP), speed sensor, potentiometer for desired speed adjustment, and switches for user interface. The desired speed is entered by the user via the potentiometer andthen entered to DSP via analog to digital converter (ADC). The speed of the motor (i.e. vehicle) is monitored using tachometer.

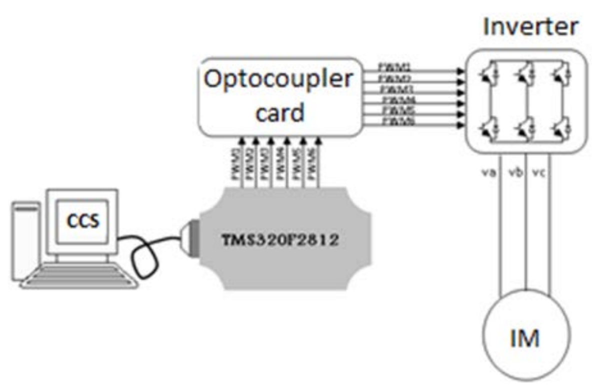

Figure4:The block diagram of the open loop control system.

6 Hardwareand Software Specifications:

6-1 Digital Signal Processor (DSP):it isa 32-bit 150MIPS TMS320F2812 DSP developed by Texas Instruments Inc. The most widely used Code Composer Studio (CCS) developed by TI is selected to program the DSP to generate PWM signals. The CCS disposes of Digital Motor Control (DMC) library which reduces significantly the time and effortrequired for programming the DSP[8]. The

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DMC library provides software modules which are dedicated for motor control. The main software modules used in our project are:VHz_PROF, SVGEN_MF and PWMGEN.

6-2Isolation Card it is used:to ensure the necessary galvanic isolation between DSP and power inverter. The card is realized using HCLP 2601 rapid optocouplers. In addition to the galvanic isolation, the card realized provides also signal inversion and amplification (Figure 5)

6-3IGBT-based Three Phase Inverter: It is an International Rectifier's IRAMY20UP60B type 20A, 600V Integrated Power Hybrid IC (HIC) with Internal Shunt Resistor for motor drives applications.

It is a compact, high performance AC motor-driver in a single isolated package which simplifies design.A built-in temperature monitor and over-current and over-temperature protections, along with the short circuit rated IGBTs and integrated under-voltage lockout function, deliver high level of protection and failsafe operation. Using a single in line package with heat spreader for the power die along with full transfer mold structure minimizes PCB space and resolves isolation problems to heat sink [12]

6-4Three Phase Squirrel Cage induction Motor

4.7 KW, 3 phase, 220/380V, 11/19A, 1500 rpm, eightLead Acid gel-type DC batteries(12v/48Ah) and fivesolar panels(500w/120v).

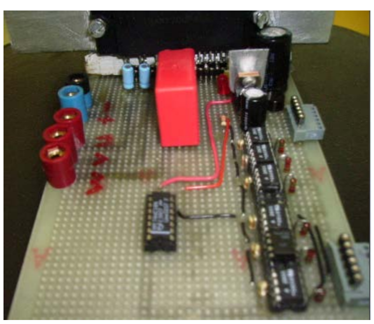

Figure 5 Galvanic isolation card realized

7 Open Loop Control Strategy

The user adjusts the desired speed using a potentiometer and this latter converts it to its analogous voltage. The output of the potentiometer is sensed by the ADC which is integrated on the DSP and then converted to desired frequency F_s. The open loop control program consists of several stages as shown in the flow chart depicted in figure6. Based on the figure, the open loop system can be summarized as follows:

- Initialization DMC modules and declare variables
- Determine V_s voltages with constant V/F profilebased on desired frequency (F_s) using VHz_PROF module.
- Determine the time durations Ta, Tb and Tcbased on V_s and $F_s$using SVGEN_MF module.
- Generate the signal PWM based on the time durations Ta, Tb and Tc using PWMGEN module.

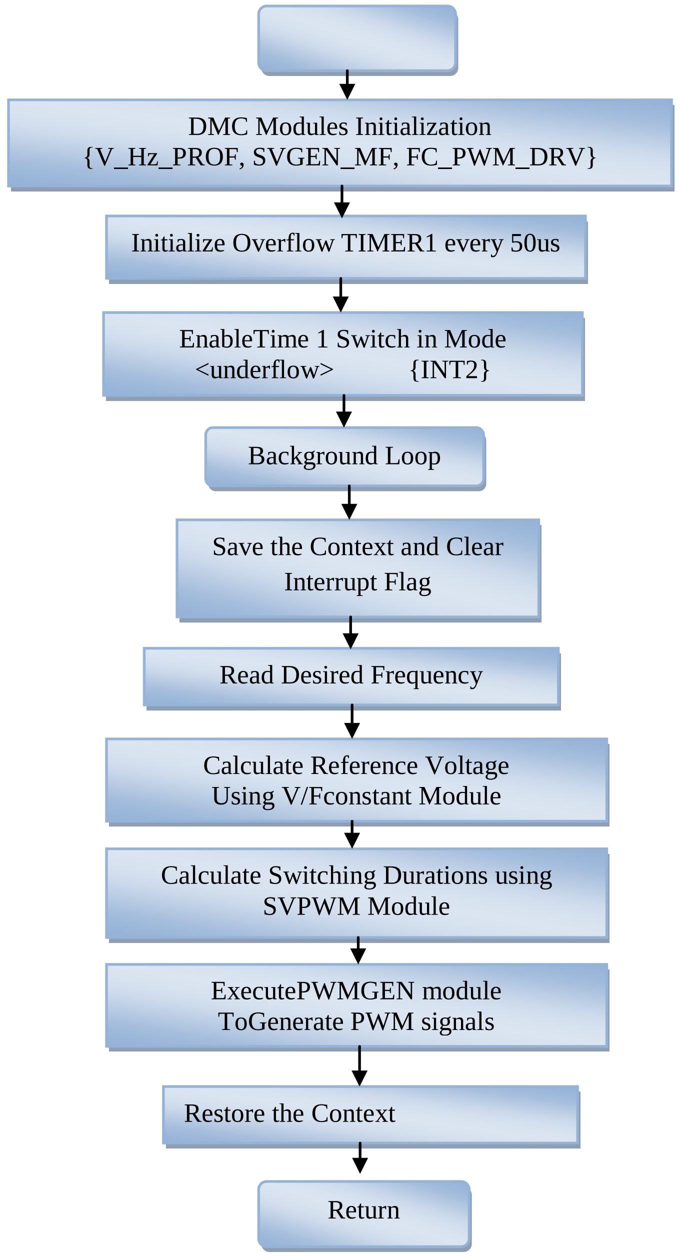

Figure 6: Program Flow Chart

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8Practical Results:

Figure7 shows the PWM signals generated by the SVPWM module after the execution of the program implemented in the DSP. Figure8illustrates the two PWM pulses which are complementary and used to trigger the gates of one leg of the IGBT Bridge of the inverter. As shown in figure8, in order to avoid the short circuit of inverter power supply, we introduced a time delay of 0.5 µs between the two complementary pulses.

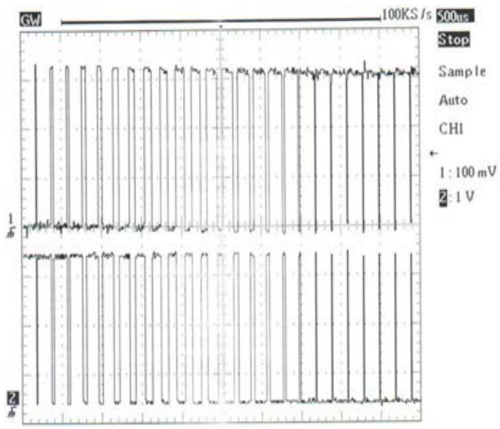

Figure 7:PWM signaland its complement.

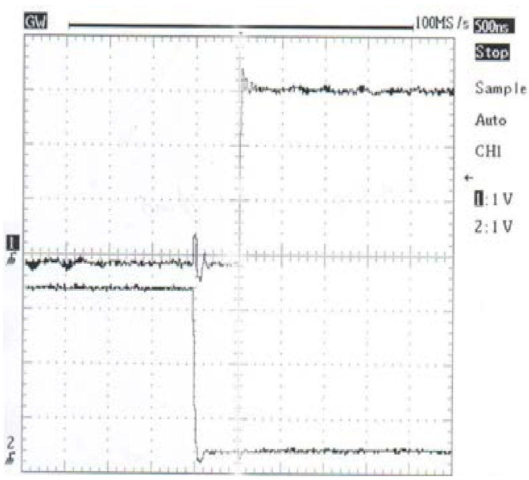

Figure 8: Dead timebetween two complementarypulses.

Figure 9 shows PWM signals before and after the optocoupler card which ensures galvanic isolation between DSP and Inverter. As shown in figure 9, the PWM signals of magnitude 3.3 volts generated at the DSP outputare inverted and amplified to 5 volts by the optocoupler card before inputting them to the inverter.

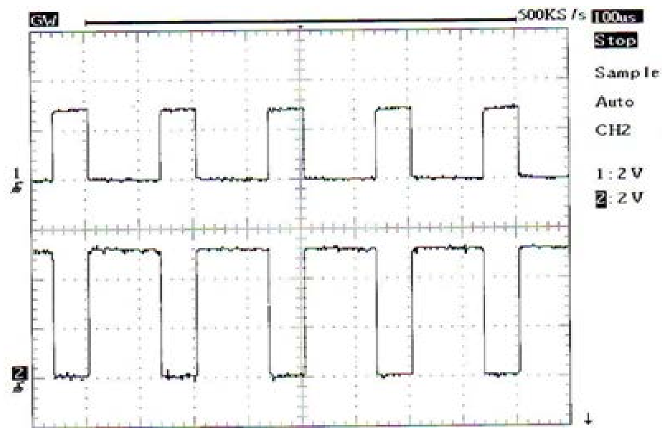

Figure 9:PWMsignalsbefore and afteroptocouplers.

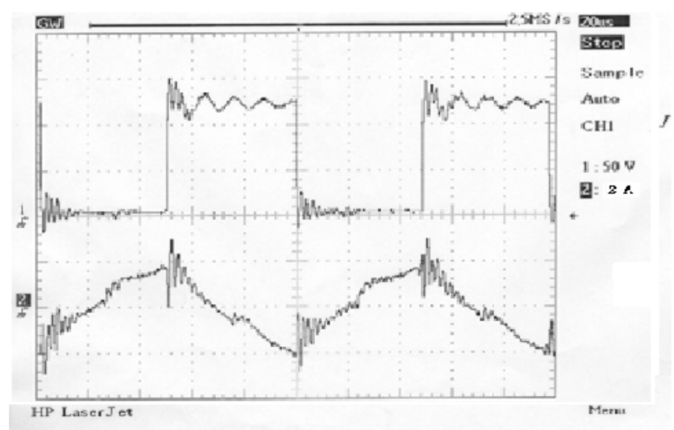

Figure10: Current waveformandvoltage waveformattheswitchingof a cell.

To check the switching behavior and the reliability of the inverter (i.e. IR IRAMY20UP60B module), we investigated the operation of one of its cell during commutation. Figure 10 illustrates the waves of current and tension for an IGBT cell under RL inductive load with R=8.4 Ω and L=4.75 mHduring commutation. The switching frequency of the IGBTs transistors and DC power supply voltage are 10 kHz and 160 V respectively. As shown in figure 10, the current increases in continuous form from 0 to 5 A during switching off (Switch Open) and then decreases back to 0 A during switching on (Switch Close). The voltage across the switch is equal to the DC power supply. Figure 10shows small currentspikes and voltage ringing during switching which are probably due to the IGBTs internal parameters.

The inverter is tested to supply induction motorwith rating 4.7KW with and without load. This motor is the one selected to be used in the propulsion system designed. The switching frequency of the IGBTs transistors and DC power supply voltage are 10 kHz and 200 V respectively. Results illustrated in figure 11 and 12 show the current and line to neutral voltage at the inverter output when supplying the motor. As can be noticed, the results are very satisfactory and the current wave is almost sinusoidal. Figures11 and 12 also show the ability of the inverter changing speed of the motor (i.e. Vehicle) by generate sinusoidal voltage for different desired frequencies (i.e. 25 Hz and 50Hz).

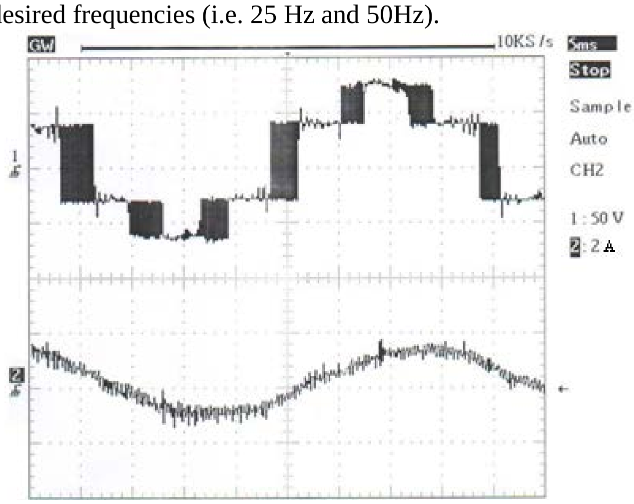

Figure 11: waveform ofthe phase voltageand currentfor f =25Hzwith aload torque.

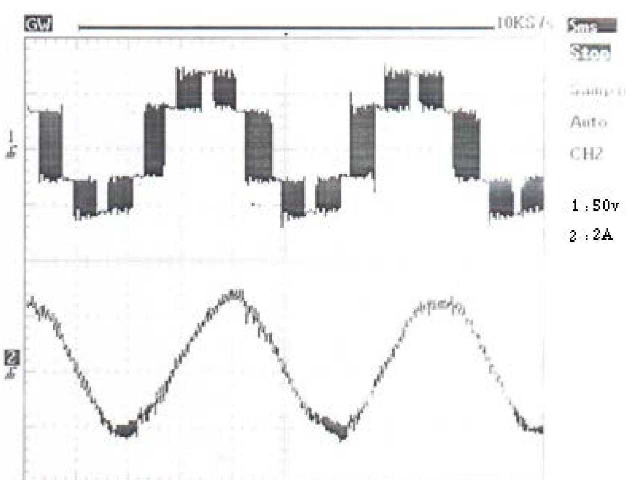

Figure12:waveform ofthe phase voltageandcurrentfor f =50Hzwith aload torque.

Finally, we investigated the practical performance of the electric propulsion system designed under road load. The vehicle has been operated on flat road and we started changing its speed at different stages. The results obtained are very satisfactory as shown in **figure 13**. The speed is increased progressively by the driver and the maximum speed reached is more than 60 km/h (i.e. 19.5 m/s) and the current required at this speed is 3.5A. The results show that the vehicle can reach speed up to 90 km/h. However, driving at this speed resulted in lot of vibrations of the vehicle. This is probably due to the incomplete design requirements of the vehicle body [11].

The capability of the electric propulsion system under overload was also investigated by operating the vehicle on graded road condition where the road grade angle is about 45 degree. The results are shown in **figure 14**. The speed reached in this case is about 12.7 m/s (i.e. 45 km/h) and the current required is 5.8 A.

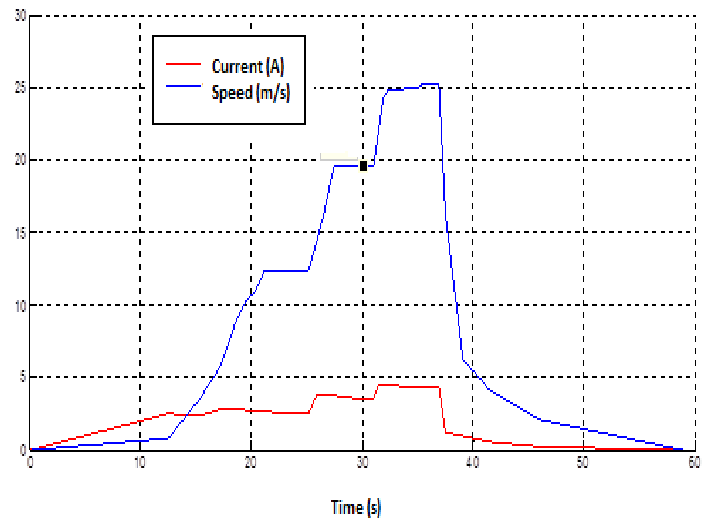

Figure 14: Running the vehicleinflat road.

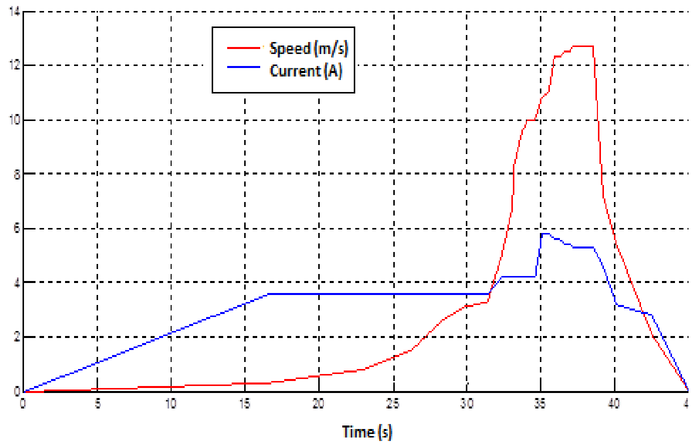

Figure 14: Running the vehicleina graded road.

9 Conclusions

The paper presents design of a battery electric vehicle which is propelled by three phase cage induction motor and powered by solar energy station. After several experiment performed, we demonstrated that the DSP-based control system developed is able to operate the vehicle at different speeds under flat and uphill road condition. However, during uphill condition the current required was quite high compared to current supplied to DC motor used on the same vehicle under the same condition. Therefore, to be comparable to DC motor, more research work is required on control strategies in order to improve the performance of induction motor used in EV.

Due to its low cost, robustness, high reliability and free from maintenance, automobile industry will certainly select cage induction motor as the most appropriate candidate for EVs [3]. Hence, we believe that the work carried out will contribute in development of future electric vehicles based on cage induction motor.

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VLSI Implementation of an improved multiplier for FFT Computation in Biomedical Applications

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***Abstract*—Discrete Fourier Transform (DFT) is a fundamental Digital Signal Processing domain transformation technique used in many applications for frequency analysis and frequency domain processing. Fast Fourier Transform (FFT) is used for signal processing applications. It consists of addition and multiplication operations, whose speed improvement will enhance the accuracy and performance of FFT computation for any application. It is an algorithm to compute Discrete Fourier Transform (DFT) and its inverse. DFT is obtained by decomposing a sequence of values into components of different frequencies. FFT can compute DFT in O(N log N) operations unlike DFT computation that takes O(N2) arithmetic operations . This reduces computation time by several orders of magnitude and the improvement is roughly proportional to N / log N. Present day Research focus is on performance improvement in computation of FFT specific to field of application. Many performance improvement studies are in progress to implement efficient FFT computation through better performing multipliers and adders.**

Electroencephalographic (EEG) signals are invariably used for clinical diagnosis and conventional cognitive neuroscience. This work intends to contribute to a faster method of computation of FFT for analysis of EEG signals to classify Autistic data.

Keywords—FFT, Multiplier, EEG

I. INTRODUCTION

Modern applications are demanding high speed computations. Technology is coming close to theoretical limits on how fast computations can be done on a single chip. Multiple processors operating in parallel, performing different functions of a process and combining them at the end is the solution to this. Fourier Transform is the basis of many signal processing and communication applications. It is the tool for analysis of the signal in its frequency domain. Fourier transform has many applications, in fact any field of physical science that uses varying signals, such as engineering, physics, applied mathematics, and chemistry, will make use of Fourier series and Fourier transforms. Most of these fields nowadays make use of digital and discrete data. Thus the determination of Fourier Transform of discrete signals is of prime importance and such a transform is called Discrete Fourier Transform (DFT). Fast Fourier Transform (FFT) is an efficient algorithm to evaluate DFT.

Discrete Fourier Transform has a wide range of applications. It is mainly used for converting discrete time domain signals to its frequency domain. However, the process of conversion is expensive and takes lot of time. Thus we go for Fast Fourier Transform which uses a divide-and-conquer approach to reduce computational complexity of DFT. DFT is defined as

$$X(k) = \sum_{n=0}^{N-1} x(n).W_N^{nK} \tag{1}$$

where n,k € [0,N-1] and $W_N^K = e^{-j2\Pi k/N}$ is the twiddle factor, x(n) is the nth sample of discrete time signal and X(k) is its frequency sample at kth instant.

Complexity of computation of DFT is O (N^2) unlike the computation of FFT which is O (N log N) butterfly operations. Hence DFT computation takes more time and is a costlier process. FFT algorithm deals with these complexities by exploiting regularities in the DFT algorithm. Radix-2 Algorithm is a common factor algorithm for N-point DFTs, where N is a power of 2. FFT computation in Radix-2 system takes place in $\log_2 N$ different steps, hence it enables pipelining in hardware design.

FFT computation involves addition and multiplication operations. As multipliers are slow performing hardware units, their performance directly affects the performance of the FFT hardware. Existing hardware multipliers are Serial Multiplier, Array Multiplier, Booth Multiplier, Wallace Tree Multiplier, Booth encoded Wallace tree multiplier, etc. Studies on performance optimizations of Booth Multiplier, Wallace Tree Multiplier and Booth encoded Wallace Tree Multipliers are in progress. Improvement in terms of Hardware Description Language (HDL), Floor planning, Routing, etc. are of main interest to Researchers. This work intends to compare the performance of main hardware multipliers and study and implement the most efficient multiplier for FFT computations in biomedical field.

FFTs are extensively used in data compressions, filtering signals, Signal spectral analysis, Image Processing, etc. In

Biomedical field, Medical Imaging plays an important role for diagnostics of various health conditions. Electroencephalography (EEG) and electrocardiography (ECG) are various techniques to study the patterns of signals generated by brain and heart, respectively. These are further researched to clinically study human behaviour and heart functions. This work analyses spectral components of EEG signals and proposes an effective method to classify EEG levels of Autistic children.

II. Fast Fourier Transform Algorithm

Fast Fourier Transform is an algorithm to compute Discrete Fourier Transform which diminishes the number of computations for n-point radix from N^2 to N logN arithmetic operations. There are two methods to compute DFT through FFT algorithm, namely, Decimation-in-time (DIT) and Decimation-in-frequency (DIF) FFT algorithms. In Radix-2 DIT-FFT, input signal is decimated into even-indexed and odd-indexed values such that the series x(n) where, n=0, 1,2,…N changes to x(2r) and x(2r+1) where r=0,1,2,….N/2-1. In Radix-2 DIF-FFT, the x(n) series is broken into x(n) for n=0,1,2….N/2 -1 and x(n) for n=N/2, N/2+1,….N-1.

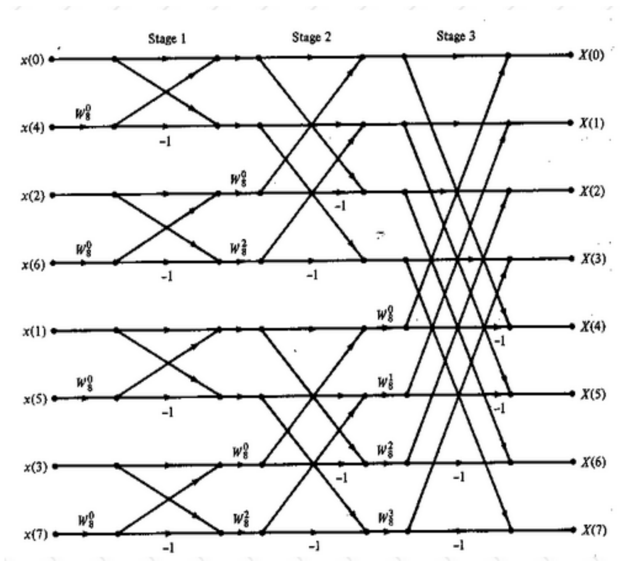

Fig. 1. Radix-2 8-point DIT-FFT algorithm

Fig. 1 shows the butterfly structure of an 8-point Radix-2 DIT-FFT algorithm. Eight time-domain inputs, namely, x0, x1, x2, x3, x4, x5, x6, x7 are transformed to their frequency components, namely, X0, X1, X2, X3, X4, X5, X6 and X7 in three stages. This paper implements Radix-2 8-point DIT-FFT algorithm.

III. Multipliers

Multipliers have large area, long propagation delays and consume power. Therefore, low-power multiplier design has an important role in design of low-power VLSI systems. Power refers to number of Joules dissipated over a certain amount of time whereas energy is the measure of the total number of Joules dissipated by a circuit [9]. In digital CMOS design, the well-known power-area/power-delay product is commonly used to assess the merits of designs [9].

Any multiplier design involves 3 steps. They are i) partial product generation ii) partial product reduction and addition iii) final addition. The partial products are formed first either by using an algorithm or using AND gate for each bit of the multiplier with each bit of the multiplicand. The next step is reduction of these partial products. The third step is addition of the remaining partial products to yield the final product [9].

Hardware multipliers widely used are Booth Multipliers and Wallace Tree Multiplier. Area and Power parameters of Booth Multiplier and Wallace Tree Multiplier are studied and their advantages have been incorporated to develop the concept of Booth-encoded Wallace Tree Multiplication.

A. *Booth Multiplier*

Booth Multiplier implements Booth Algorithm, named after its originator, A. D. Booth. This algorithm is implemented for signed multiplication of integers and can be extended to real numbers. Algorithm is based on recording the multiplier to a recorded value leaving the multiplicand unchanged [6] i.e.

• Each ‘0’ digit is retained in the recorded number until 1 is encountered on evaluating from LSB to MSB.

• Complement of 1 is inserted at every ‘1’ digit in recorded number and all other succeeding 1’s are complemented until a ‘0’ is encountered.

• Then, replace the ‘0’ with ‘1’ and continue the process.

Two main drawbacks of Booth Algorithm are the inefficiency of the circuit when isolated 1’s are encountered and difficulty in designing parallel multipliers as number of shift-and-add operations may vary. Hence Modified Booth Algorithm was developed by O. L. Macsorley. Modified Booth Algorithm is twice as fast as normal Booth Algorithm [4]. This modified Booth Encoding algorithm reduces the number of partial product rows to (N +2)/2 where N is the number of bits of Multiplier or Multiplicand [4].

B. *Wallace Tree Multiplier*

Wallace Tree Multiplier is one of the hardware multipliers used to accomplish high speed and low power multiplication to condense the number of partial products generated. There are two main techniques followed in designing Wallace Tree Multiplier. First technique is to consider all bits in each column at a time and compress them into two bits, namely, Sum and Carry. Second technique is to consider all bits in four rows at a time and compress them. Wallace Tree Multipliers use half adders, full adders, 4:2 and 3:2 compressors and a high speed adder [10].

Partial product generation, partial product addition and final addition are the three stages in a multiplier. In Wallace Tree Multiplier, the multiplicand is multiplied by the multiplier, bit-by-bit, to generate partial products. They are, then, added based on Wallace Tree structure to produce two rows of partial products which are finally added using any high speed adder. The critical path delay of Wallace Tree multiplier is proportional to the logarithm of the number of bits in the multiplier [9].

Algorithm for Multiplication of two signed integers is as follows:

• Multiply (AND) each bit of one of the arguments,

• Reduce the number of partial products to two by layers of full adders and half adders (Compressors).

• Group the wires in two numbers, and add them with a conventional adder [9].

Wallace tree multiplication can be implemented only for signed integers and are avoided for low power applications as excess wiring consumes more power.

C. Booth-Encoded Wallace Tree Multiplier

Based on the comparative study of Area and Power parameters of Booth Multiplier and Wallace Tree Multiplier, Booth-encoded Wallace Tree Multiplier is chosen as an efficient multiplier for FFT computation. Table I. shows Area and Power performance parameters of the two multipliers which are coded in Verilog HDL and performance parameters are evaluated using IC Compiler tool from Synopsys Inc. Though Wallace Tree multiplier shows better performance in terms of Area and Power than Booth multiplier, its operation is limited to signed integers alone. As FFT computation in biomedical applications involve signed real numbers, Booth Algorithm is to be implemented for the multiplier.

TABLE I. PERFORMANCE PARAMETERS OF 4X4 BOOTH MULTIPLIER AND WALLACE TREE MULTIPLIER

Multiplier	Area(nm^2)	Power(μW)
Booth Multiplier	974.872	235.184
Wallace Tree Multiplier	600.868	180.504

Multiplication of the two operands, Multiplicand (MD) and Multiplier (MR) results in 2N bits for conventional multiplication. However, Booth encoded multiplier reduces number of partial products to (MD/2 -1) partial products [5]. Booth Algorithm is based on recording the multiplier to a recorded value leaving the multiplicand unchanged. It scans the multiplier operand and skips chains. It reduces the number of additions required to produce the result [4]. Booth-encoded Wallace Tree Multiplier has advantages of both Booth Multiplier and Wallace Tree Multiplier. This paper implements Booth encoding to increase speed of algebra by reducing number of partial products and Wallace Tree module for decreasing number of levels of addition.

1) Architecture of the Multiplier

In Booth encoded multiplier, number of partial products are reduced by grouping multiplier bits into pairs and selecting partial products from the set {0, M, 2M, 3M} where M is the multiplicand. Modified Booth encoded multiplier, avoids the use of Carry Propagate Adder to calculate 3M, rather it utilizes Carry-Save-Adder. Thus, in Modified Booth Algorithm, number of partial products is reduced by a factor of two without a pre-adder to produce partial products [6]. Multiplier decoding is done such that multiples needed are in {0, M, 2M, 4M + -M} data set. These multiples can be generated using shift-and-complement methods.

Fig.2 shows the architecture of Booth-encoded Wallace Tree Multiplier which consists of five blocks, namely, 2's Complement Generator, Booth Encoder, Partial Product Generator, Wallace Tree module and Carry Look-ahead Adder [7]. Booth encoder inspects each bit of the multiplicand and records the multiplier in terms of 0, 1 and complement of 1. As complement of 1 cannot be represented on hardware, operational equivalent of recorded multiplier is implemented based on Table II. Here, outputs of the encoder. x and z are defined as:

$$x = MR[i] \bullet MR[i-1] \quad (2)$$

$$z = MR[i] \oplus MR[i-1] \quad (3)$$

Where MR[i] and MR [i-1] corresponds to i^{th} and $i\text{-}1^{th}$ bit of Multiplier, respectively. 2's complement generator takes the multiplicand MD as input and produces –MD as output .i.e. inverts all bits of multiplicand and uses a Ripple Carry Adder to generate 2's complement. Partial product generator generates appropriate partial products to be added in Wallace tree structure. Wallace Tree module adds all partial products. Addition is implemented using Carry Look Ahead Adder [7].

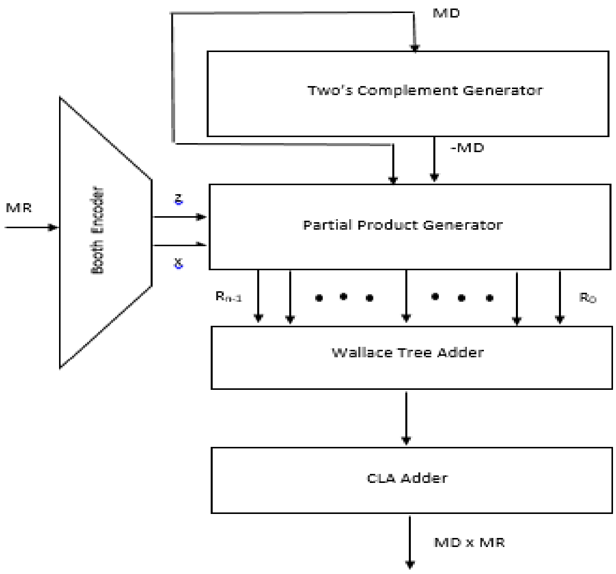

Fig. 2. Booth-encoded Wallace Tree Multiplier

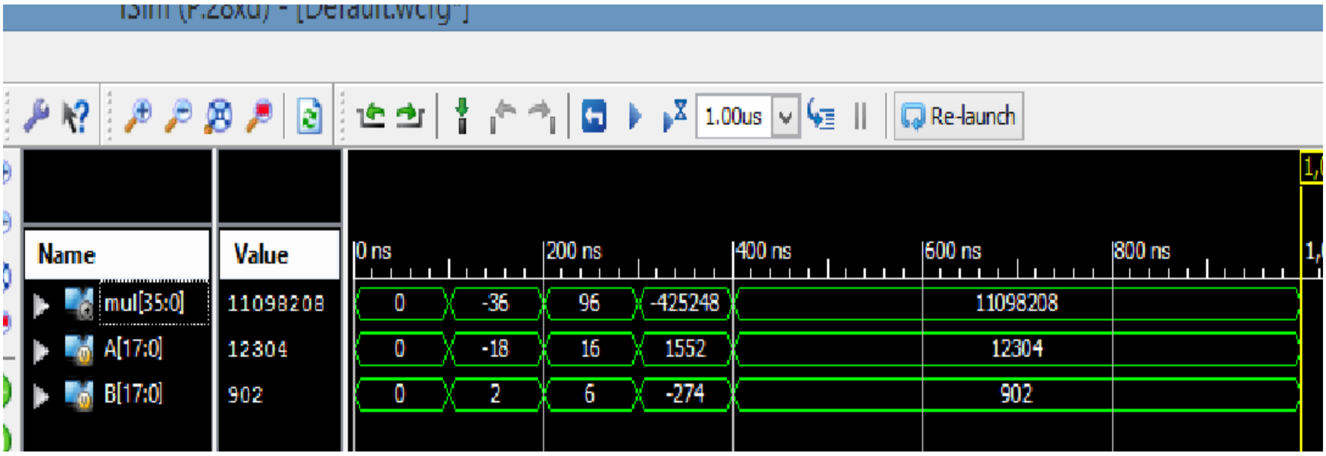

Fig. 3. Simulation Results of Booth-encoded Wallace Tree Multiplier

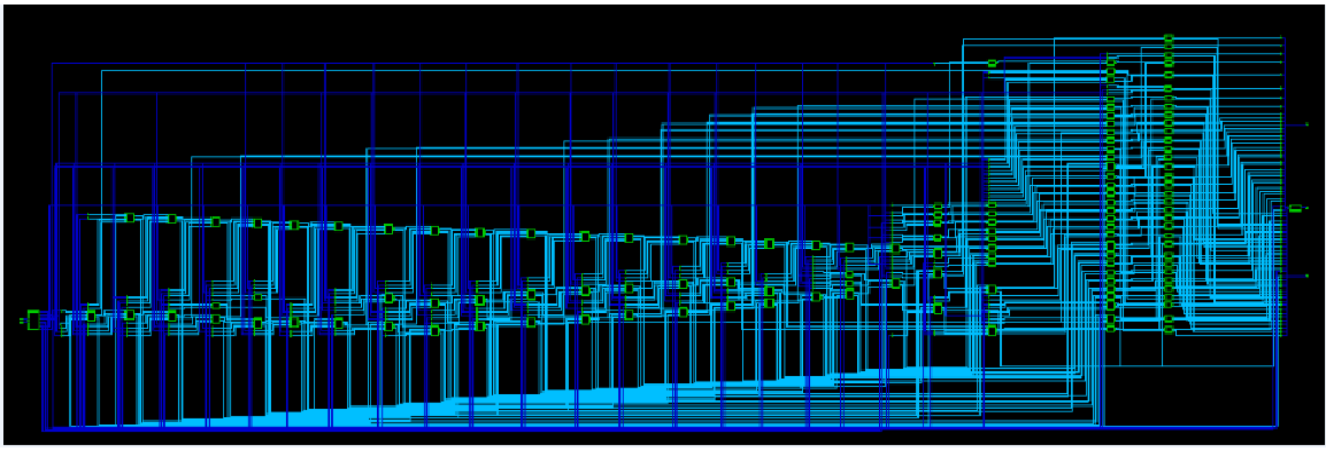

Fig. 4. Generic Gate-level Schematic of Booth-encoded Wallace Tree Multiplier

TABLE II. BOOTH ENCODING VALUES

MR[i]	MR[i-1]	Recorded y[i]	x	z	Assigned to partial product
0	0	0	0	0	0
0	1	1	0	1	MD. sign extended
1	0	$\bar{1}$	1	1	-MD, sign extended
1	1	0	0	0	0

Hardware Description Language (HDL) implementation of Booth-encoded Wallace Tree Multiplier has been done in Verilog HDL. The outputs are correctly obtained for both signed and unsigned multiplication. Simulation has been done using Xilinx ISE tool. Generic Gate-level schematic has been obtained in IC Compiler tool from Synopsys Inc. Fig. 3 and Fig. 4 show the simulation results and Generic Gate-level Schematic of the Booth-encoded Wallace Tree Multiplier.

IV. FFT WITH BOOTH-ENCODED WALLACE TREE MULTIPLIER

FFT implementation using Booth-encoded Wallace Tree Multiplier is an efficient circuit with advantages of both Booth Multiplier and Wallace Tree Multiplier. As explained in II, Modified Booth Algorithm is used to calculate Partial Products as per Table II. Partial Product Generator provides minimum number of partial products which are added using Wallace Tree structure. Hence, efficient algorithm of multiplication is implemented.

Radix-2 8-point DIT-FFT has been coded in Verilog HDL for input values scaled up by a factor of 10000. There are ten inputs to the circuit, namely, eight time-domain samples, Twiddle factor 'wr' and the scaling factor 'k'. Outputs are separately obtained for real and imaginary parts of corresponding frequency components.

As 8-point corresponds to 3 stages ($8 = 2^3$), twiddle factor varies for each stage. Twiddle factor is calculated as in (1). For N=1, Twiddle factor value is {1}, for N=2, Twiddle factor values are {1, -j} and for N=3, Twiddle factor values are {1, -j, $(1/\sqrt{2}) - j(1/\sqrt{2})$, $(-1/\sqrt{2}) - j(1/\sqrt{2})$}. Depending on the accuracy of outputs required, scaling can be varied from 10 to any power of 10 and by increasing the number of significant digits of twiddle factor value of $(1/\sqrt{2})$. Simulation results shown in Fig.5 has been scaled up for a factor of k = 10000. Outputs and inputs have been correctly verified. Accuracy of $\pm 0.1\%$ is obtained for scaling improvement from 1000 to 10000.

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Design Vision tool from Synopsys Inc. is a logic synthesis tool which inputs HDL design and synthesize out gate-level HDL net lists. Fig. 6 shows the Generic Gate-level schematic diagram implemented in 90 nanometer technology using saed90nm_typ_ht.db library in IC Compiler tool from Synopsys Inc.

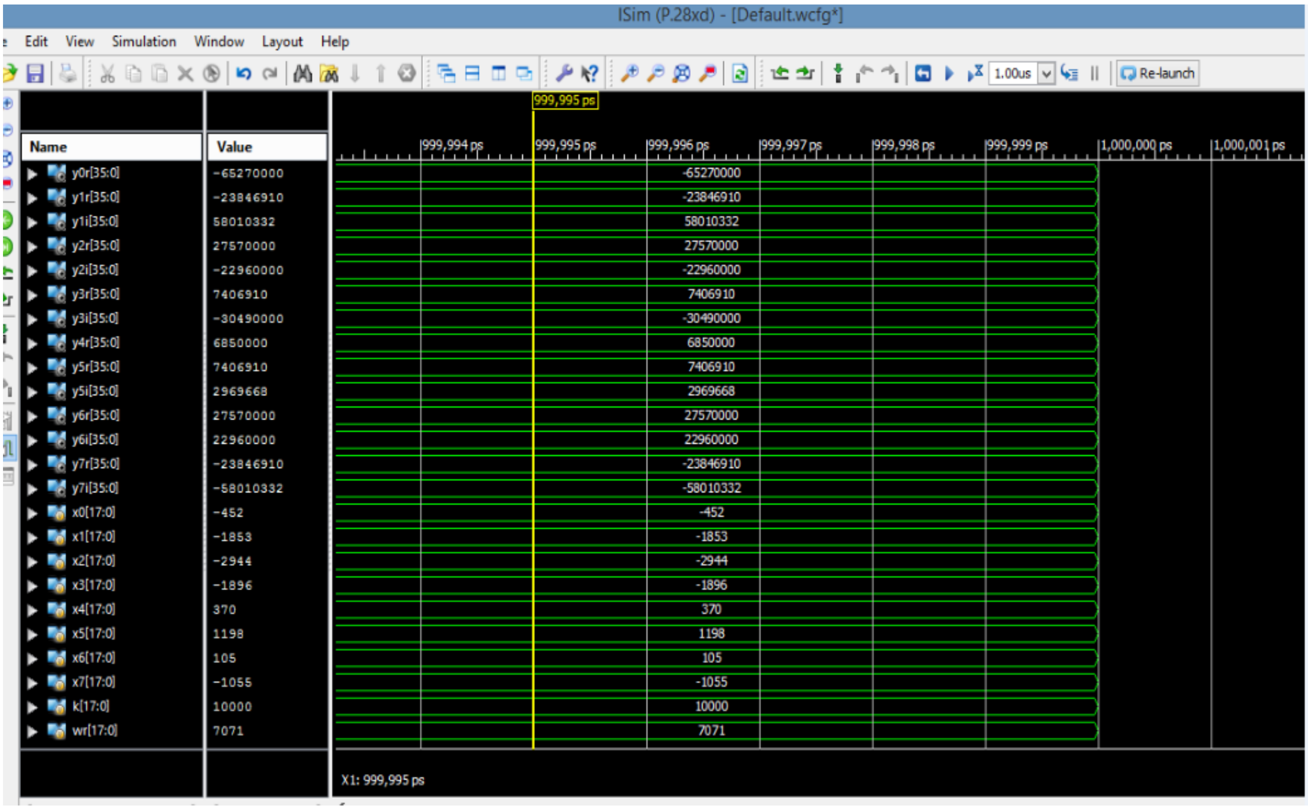

Fig. 5. Simulation Results of FFT with Booth-encoded Wallace Tree Multiplier shown in Signed Decimal Radix

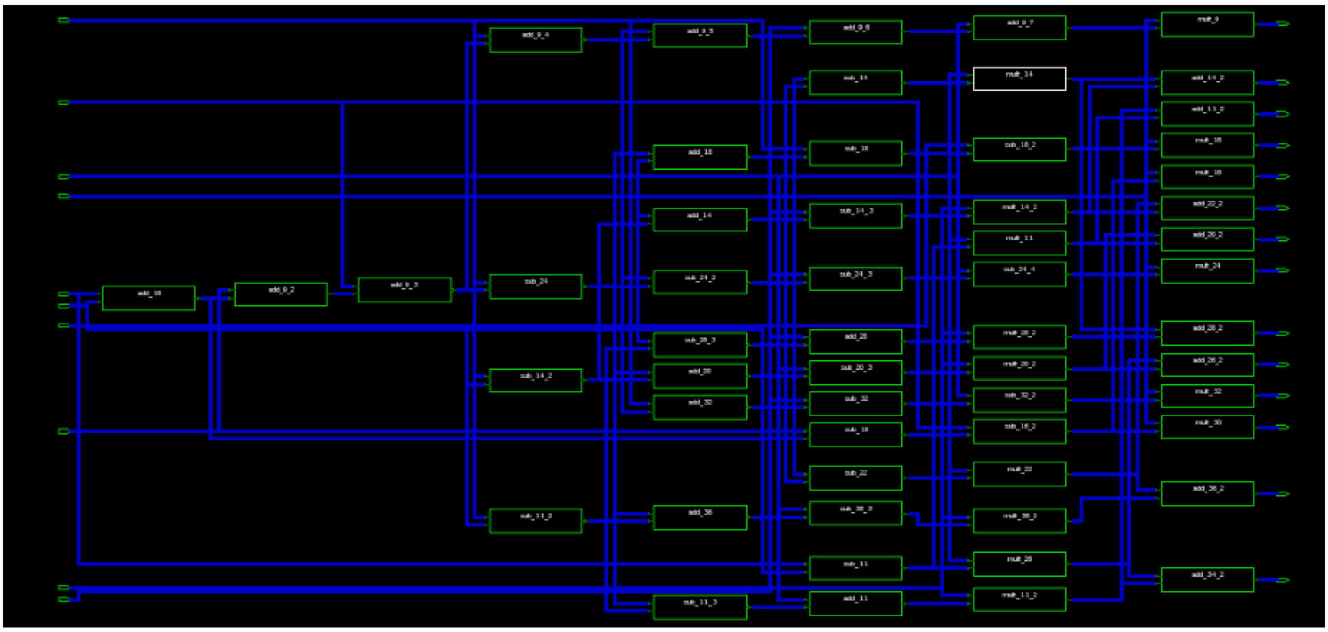

Fig. 6. Generic-Gate level Schematic of FFT with Booth-encoded Wallace Tree Multiplier

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V. FFT AND EEG

Virtually all sciences in the world contribute to the maintenance of human health and the practice of medicine. Medical physicists and biomedical engineers support the effective utilization of this medical science and technology as their responsibilities to enhance human health care with the new development of the medical tools such as Electroencephalogram. Electroencephalography (EEG) is a mechanism of measuring electrical activity of the brain. Upon studying EEG signals, various health conditions can be monitored and diagnosed e.g. Brain diseases like Alzheimer, Tumors, Head injuries, Epilepsy, Dementia, Human Behaviour, etc. These signals are recorded from various positions on scalp through electrodes and conductive media. Diagnostic results are made from the spectral content of EEG signals. Here comes the importance of FFTs in EEG signal analysis. They are extensively used in neuroscience, cognitive science and cognitive psychology due to its capability to reflect both normal and abnormal electrical activity of brain [1].

EEG signals are typically represented either through rhythmic activity or transients. Rhythmic Activity of brain signals is divided into different bands of frequency, namely, Delta, Theta, Alpha, Beta, Gamma. Table III. shows the frequency range of each band and the different states of the person [1]. Amongst these bands, Alpha band is widely used for various diagnostic studies [8]. Real-time applications like alerting drivers about their drowsiness through EEG variations in Alpha band is one of its kind. EEG signal analysis are crucial for evaluating Epilepsy. In marketing field, EEG signals have been used to study customer response to various products in market as a feedback method and product improvement study, referred to as neuro-marketing.

TABLE III. FREQUENCY BANDS IN EEG SIGNAL

EEG bands	Frequency band(in Hz)	Prominent
Delta	Less than 4	Deep sleep
Theta	4-7	Drowsiness
Alpha	8-13	Relaxed and awake
Beta	14-30	Sleep stages
Gamma	>30	Finger movements

In this work, EEG signal analysis is used to classify EEG levels of Autistic persons in Alpha band. Autism is a brain development disorder whose symptoms are visible since childhood. Autistic children due to seizures, show high delta and theta waveforms and low alpha waveform due to less metabolism. EEG signal pattern of normal persons are similar for similar age group, sex, race, food habits, environmental conditions, etc. However, frequency bands will remain the same for all people. Different types of special children show variations in EEG signals in Alpha band depending on their neurological function. Hence they can classified by comparing values of mid-frequency Alpha band of normal and Autistic persons.

EEG samples have been collected for a normal male aged at 21 years during closed eye condition based on 10 – 20 International Standards Electrode System with 19 channel electrode placement and 1 electrode as reference. FFT is computed for the two Occipital electrode position (O1 and O2) samples at a sampling frequency of 80 Hz in MATLAB. Power Spectral response is obtained to study and analyze Alpha band. Similarly, Radix-2 8-point DIT-FFT computation is performed using FFT implemented through Booth-encoded Wallace Tree Multiplier for the same sample.

Mid-frequency FFT value of Alpha band, at 10 Hz, are compared for the normal person. Values obtained through MATLAB and the FFT implemented circuit using Xilinx ISE is given in Table IV. Real-part values of the computed FFT at electrode O2 are plotted in Fig.7. Y-axis corresponds to real value of computed FFT and X-axis shows the corresponding frequency. Value at X0 = -0.0006527 volts is also shown in the figure.

TABLE IV. VALUES OF 8-POINT FFT FROM MATLAB AND XILINX ISE

Out-put	FFT using MATLAB (O2 electrode position) x 10^{-3} volts	FFT computed using VLSI circuit (O2 electrode position) x 10^{-11} volts
X0	-0.65257216 + j0.00000000	-65270000 +j0
X1	-0.23850908 + j0.58005815	-23846910 + j58010332
X2	+0.27570022 - j0.22963366	+27570000 - j22960000
X3	+0.07405211 - j0.02970924	+7406910 - j2969668
X4	11+0.06849303 + j0.00000000	+6850000+ j0
X5	+0.07405211 + j0.02970924	+7406910 + j2969668
X6	+0.27570022 + j0.22963366	+27570000 + j22960000
X7	111`-0.23850908 - j0.58005815	-23846910 – j58010332

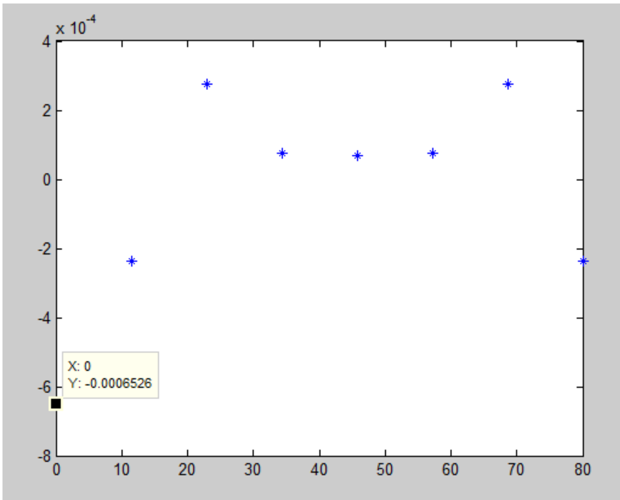

Fig. 7. Real-part values of the FFT output from MATLAB

VI. Results and Discussion

EEG data collected for a normal person has been sampled at 80 Hz in MATLAB. Delta band value X0 has been obtained as -0.0006526 volts. FFT has been implemented using Booth-encoder Wallace Tree multiplier to compute Radix-2 DIT-FFT algorithm. The same sample has been given as input to the FFT circuit in Test bench and delta band value is obtained as (-65270000 x $10^{-11)}$ volts. An accuracy of $\pm 0.019\%$ has been obtained through the implemented FFT circuit for all eight outputs obtained.

As per [1], Alpha band value of Autistic child is less than that of a normal child. The implemented FFT algorithm can be used to verify this result. Accuracy of computed Fast Fourier Transform value can be increased by increasing the significant digits of the twiddle factor ($1/\sqrt{2}$). The results obtained show an improvement in accuracy of +0.019% for four decimal places of twiddle factor ($1/\sqrt{2}$). Complexity of the circuit increases with increase in width of data.

VII. Conclusion and Future Scope

Generic-gate level implementation of Fast Fourier Transform using Booth-encoder Wallace Tree Multiplier has been done using VLSI 90nm technology. The circuit has been studied and analyzed for data accuracy and efficient performance. An accuracy of $\pm 0.019\%$ has been obtained for four decimal places of twiddle factor ($1/\sqrt{2}$). On increasing the number of significant digits of the twiddle factor, accuracy of output can be improved but it will share a trade-off with the area of the circuit. Physical level chip design and further optimization of the circuit in terms of area and power and increasing the number of points for FFT computation form the future scope of work.

Autistic EEG samples can be evaluated for the mid-frequency alpha band. This value is expected to be lower than normal person [1]. This circuit can thus be used to classify Autistic person based on EEG level and this work can be extended for its further analysis and verification.

Acknowledgment

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Realization of Tuneable MOS-C Quadrature Sinusoidal Oscillator Using Composite Current Conveyor

Hasan Çiçekli, Ahmet Gökçen

***Abstract*—**In this paper, a new voltage-mode MOS-C quadrature sinusoidal oscillator circuit based on composite second-generation current conveyor (CCCII) is presented. The proposed topology employs two CMOS based CCCII and four grounded components. CCCII is implemented by two CCII, so it also is possible to employ the circuit by commercially available AD844 by Analog Devices. The validity of the proposed circuit has been verified by PSPICE simulation programme. Simulation is done for both CMOS based implementation and AD844 based implementation of CCCII. It is seen that the simulation results agree well with the theoretical analysis and the proposed circuit achieves a good THD performance. The resistors used in the circuit are implemented by MOS transistors. So, the proposed circuit is fully integrable and it is possible to adjust the oscillation frequency by external MOS gate voltage. Also, it is stated how the CCCII employing circuit enhance the circuit performance when compared to the same topology employing CCII.

***Keywords*—**Analog integrated circuits, Current conveyors, MOS-C realization, Oscillators.

I. INTRODUCTION

Quadrature sinusoidal oscillators find wide range of applications in telecommunication, signal processing, instrumentation, measurement and control systems and they can offer sinusoidal signals with 90° phase difference that is a requirement for some devices such as quadrature mixers, phase modulators and single-sideband generators [1]-[4]. For measurement purposes, quadrature sinusoidal oscillators are used as vector generators or selective voltmeters [5].

During recent years, several implementations of quadrature sinusoidal oscillators employing different high-performance active building blocks such as current feedback operational amplifier(CFOA), different types of current conveyor, four terminal floating nullor (FTFN), current follower, current differencing buffered amplifier (CDBA), current differencing transconductance amplifier (CDTA) and operational transresistance amplifier (OTRA) have been reported [6]-[21]. However, there is one or more drawbacks of these reported circuits such as excessive use of the passive elements, especially the external resistors, use of multiple-output active elements that makes the circuits more complicated, use of floating capacitor, which is not convenient for integration and the lack of electronic adjustment of the oscillation frequency.

The aim of this work is to present a new CCCII based quadrature sinusoidal oscillator realization and to do performance comparison to see how the CCCII based circuits have enhanced performance when compared to the same topology employing CCII. The features of the proposed circuit are as follows:

a) The capacitors and resistors used in the circuit are all grounded.
b) Resistors are implemented by MOS transistors, so the circuit is suitable for integration.
c) Electronic adjustment of the oscillation frequency.
d) Providing good characteristic with lower distortion than the oscillator circuit employing CCII.
e) Using only two active elements with single outputs.
f) Possibility to adjust the oscillation frequency without affecting the oscillation condition.
g) Possibility to employ the circuit by using commercially available AD844.

In the literature we have found, among the voltage mode quadrature sinusoidal oscillator circuits, none of them employs CCCII and have the whole features shown above.

II. CIRCUIT DESCRIPTION OF CCCII

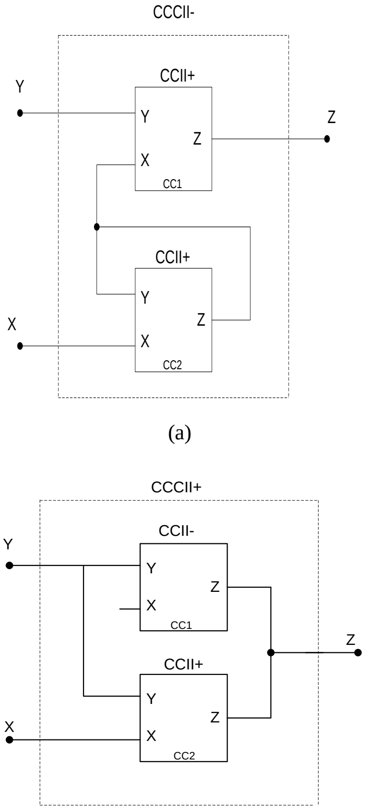
The current conveyor is still emerging as one of the most important current-mode active building block and different types of current conveyor enable the researchers to design multipurpose circuits to be used in analog signal processing. CCCII can be constructed of two second generation current conveyors as shown in Fig.1 [22]. It is a useful technique to enhance the performance of the current conveyor by either lowering the x-terminal impedance or enhancing the y-terminal admittance [22]. This provides the CCCII based circuits have better output characteristics when compared to the same circuit topology employing CCII. In the CCCII-configuration, the lower conveyor CC2 works as a negative impedance conveyor and consequently the X-terminal impedance of the CCCII- is

$$Z_{x(composite\ )} = Z_{x1} + A_{i2}Z_{x2} \cong Z_{x1} - Z_{x2} \qquad (1)$$

It is clearly seen from (1) that the current gain A_{i2} should be designed slightly lower than the first in order to prevent a negative X-terminal impedance for the composite conveyor.

In addition, all even order nonlinearities in Z_{x1} and Z_{x2} are effectively summed together and hence X-terminal impedance nonlinearity is increased. Fortunately, in most cases the nonlinearity of the X-terminal impedance has little effect on the total amplifier distortion [22].

It is possible to implement the CCCII by using the current conveyor blocks as subcircuit. This current conveyor based CCCII implementation method makes it possible to employ the circuit by using commercially available AD844.



(a)

(b)

Fig. 1 Composite second-generation current conveyor implementation using CCIIs.
(a) Composite CCII- with lower *Zx*.
(b) Composite CCII+ with enhanced *Yx*.

III. PROPOSED CIRCUIT TOPOLOGY

The proposed CCCII based voltage-mode quadrature sinusoidal oscillator topology is shown in Fig. 2.

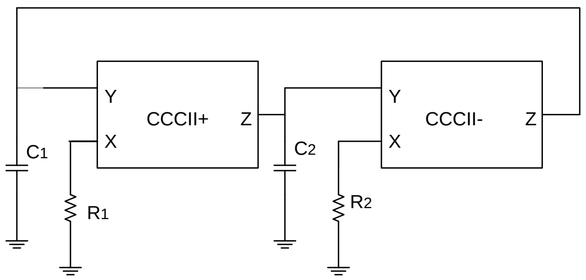


Fig. 2 Proposed circuit topology

The circuit analysis of the proposed quadrature sinusoidal oscillator yields the following characteristic equation

$$s^2C_1C_2 + G_1G_2 = 0 \tag{2}$$

The radian frequency of oscillation is

$$\omega_o = \frac{1}{\sqrt{R_1R_2C_1C_2}} \tag{3}$$

The sensitivity of radian frequency to the passive components are all calculated as

$$S_{R_1}^{\omega_0} = S_{R_2}^{\omega_0} = S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = -1/2 \tag{4}$$

As it is shown in (4), the sensitivities of passive components are quite low.

IV. MOS-C REALIZATION OF THE PROPOSED CIRCUIT

A linear resistor has been realized by using parallel connection of two depletion type NMOS transistors operated in the triode region as illustrated in Fig. 3 [23]. This method cancels out the non-linearity of the MOSFET significantly.

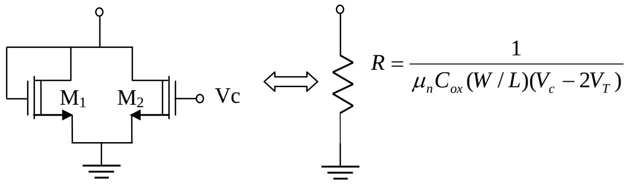


Fig. 3 Linear resistor realization using nonlinearity cancellation technique in parallel connection of two NMOS transistors

Where W and L are the channel width and length and V_T is the threshold voltage of the MOSFET, μ_n is the free electron mobility in the channel and C_{ox} is the gate oxide capacitance per unit area. The resistance values are tunable via V_C and since the even-order nonlinearities are cancelled out, it operates linearly over an extended voltage range. For achieving the fully MOS-C realization of the proposed oscillator circuit, the resistors must change with their MOS transistor conjugates.

Fig. 4 shows MOS-C realization of the proposed circuit. It is clear from this figure that the oscillation frequency of the circuit can be controlled by gate voltages V_{C1} and V_{C2} of the MOS transistors.

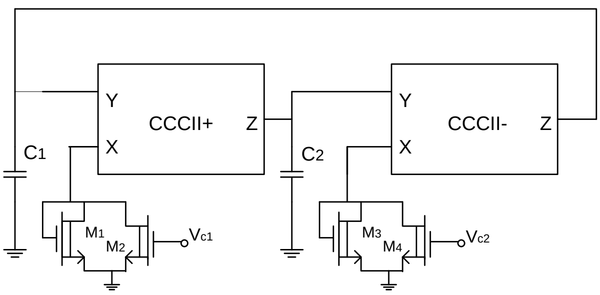


Fig. 4 MOS-C realization of the proposed circuit

V. SIMULATION RESULTS

The proposed circuit's performance has been evaluated for two different implementation of CCCII by PSPICE simulation programme using the MOSIS 0.35 µm CMOS process parameters and AD844 Macro-model parameters.

A. *CMOS Based CCCII Simulation Results*

The circuit schematic of CMOS CCII used to implement the CCCII is shown in Fig. 5 [24]. The circuit is supplied with symmetrical voltages of ±1.25 V. W/L parameters of MOS transistors used in simulation are as in [24].

The biasing currents are taken *as* $I_{B(CCII+)} = I_{B(CCII-)} = 5\,\mu A$. The passive component values taken in simulation

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are given in Table I. In the simulations, the process parameters of MOS transistors used to realize the resistors in Fig. 4, are taken as W=8.3 μm and L=0.7μm for all M1, M2, M3 and M4. MOS gate voltages are taken as $V_{C1}=V_{C2}$ =2.9 V and the resistor value is found as $R \cong 254\ \Omega$.

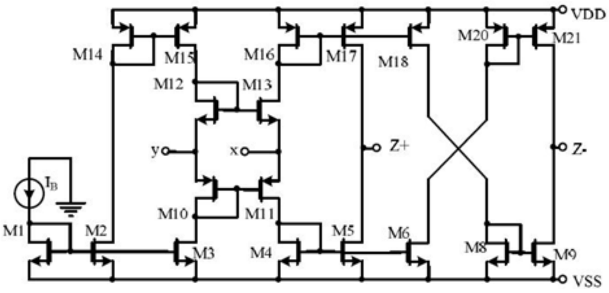


Fig. 5 Circuit schematic of dual output CMOS CCII used for CCCII implementation

TABLE I. PASSIVE COMPONENT VALUES

R_1	R_2	C_1	C_2
250 Ω	250 Ω	500 pF	500 pF

The calculated value of oscillation frequency is f_0= 1.27 MHz. In order to make a performance comparison, two simulations are done for the circuits employing CCII and CCCII. The oscillation frequency and total harmonic distortion (THD) values obtained from the simulations are given in Table II. V(1) and V(2) denote the voltages across the capacitors C_1 and C_2.

TABLE II. OSCILLATION FREQUENCY AND THD VALUES FOR CMOS IMPLEMENTATION

	Circuit employing CCII		**Circuit employing CCCII**	
Oscillation Frequency (MHz)	1.15		1.22	
THD %	V(1)	V(2)	V(1)	V(2)
	6.1	8.5	3.1	3.9

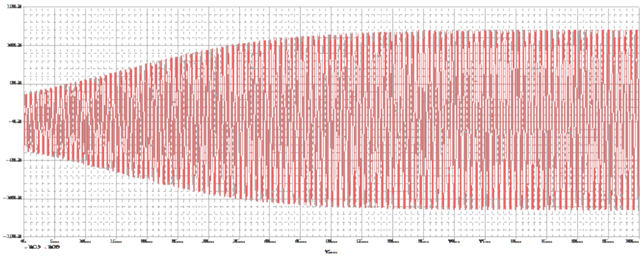
As it is seen from Table II, simulation results agree well with the theoretical calculations and the proposed circuit achieves a good THD performance. Table II also shows that the THD values of the circuit employing CCCII are significantly better than the values of the circuit employing CCII. The power dissipation of the circuit employing CCCII is 2.69 mW for the initial voltage of 0.2 mV given to C_1. The quadrature phase error is 1.98 % and the oscillation frequency deviation error is 3.93 % for the circuit employing CCCII.

In order to evaluate the tuneability of oscillation frequency, the gate voltages of M2 and M4, which are shown as V_{C1} and V_{C2}, are varied in a range of 2-3 V. The frequency values obtained by the variations of V_{C1} and V_{C2} are summarized in Table III.

TABLE III. THE OSCILLATION FREQUENCY AND THD VALUES OBTAINED BY THE VARIATION OF V_{C1} AND V_{C2}

V_{C1}, V_{C2} (V)	Oscillation Frequency (MHz)	THD %	
		V(1)	V(2)
2.0	0.87	1.0	1.7
2.2	0.96	1.6	2.5
2.4	1.04	0.9	1.3
2.6	1.10	1.0	0.8
2.8	1.19	2.1	2.4
3.0	1.26	5.4	3.7

The voltage waveforms of the proposed circuit employing CMOS based CCCII are shown in Fig.6.



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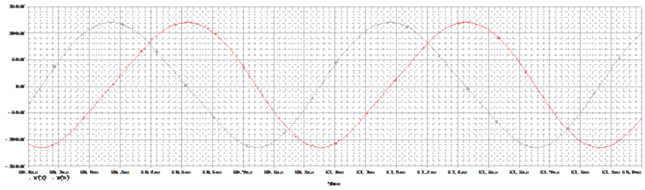

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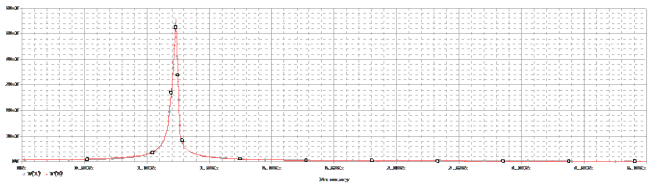

(c)

Fig. 6 Simulation results of the quadrature sinusoidal oscillator circuit by using CMOS based CCCII. (a) Initial state waveform (b) Steady state waveform (c) The frequency spectrum

B. AD844 Based CCCII Simulation Results

Another simulation is done by using the AD844 SPICE Macro-model parameters to check the workability of the presented circuit. The circuit is supplied with symmetrical ±10 V and the passive component values taken in simulation are as shown Table I. As it is done before, two simulations are done for the circuits employing CCII and CCCII. The oscillation frequency and THD values obtained from the simulations are given in Table IV.

TABLE IV. OSCILLATION FREQUENCY AND THD VALUES FOR AD844 IMPLEMENTATION

	Circuit employing CCII		**Circuit employing CCCII**	
Oscillation Frequency (MHz)	1.20		1.23	
THD %	V(1)	V(2)	V(1)	V(2)
	4.6	4.3	1.6	3.4

Also in AD844 based CCCII implementation, the THD values of the circuit are better than the values of the circuit employing CCII as shown in Table IV. The power dissipation of the circuit employing CCCII is 659 mW for the initial voltage of 0.1 mV given to C_1. The quadrature phase error is 0.64 %.

The voltage waveforms of the proposed circuit employing AD844 based CCCII are shown in Fig.7.

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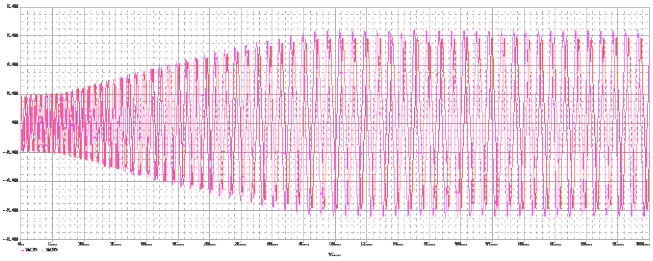
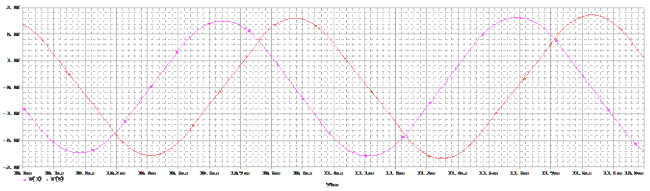


(a)



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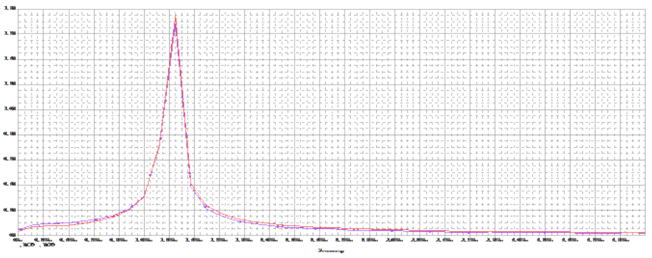

(c)

Fig. 7 Simulation results of the quadrature sinusoidal oscillator circuit by using AD844 based CCCII. (a) Initial state waveform (b) Steady state waveform (c) The frequency spectrum

VI. CONCLUSION

A voltage-mode MOS-C quadrature sinusoidal oscillator based on CCCII has been presented. The resistors used in the circuit are implemented by MOS transistors and the capacitors are all grounded. So, the proposed circuit is fully integrable and it is possible to adjust the oscillation frequency by external MOS gate voltage. The simulation results agree well with the theoretical analysis. The proposed circuit achieves a good THD performance and the quadrature phase error is quite low. It is stated that the CCCII employing circuits enhance the circuit performance significantly when compared to the same topology employing CCII. The workability of the presented circuit is also verified by using commercially available AD844. It is expected that the proposed circuit will be useful in various telecommunication and signal processing applications.

ACKNOWLEDGMENT

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Adaptive Read Voltage Control for Improvement of Read Disturbance and Power Consumption in Cross-point ReRAM

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***Abstract*—** We investigated the adaptive read voltage control as an efficient method for reducing power consumption and lowering read disturbance in Cross-point ReRAM (Resistive RAM). We propose to adjust the read voltage depending on read margin reflected cell variation analysis by using ADC. It can improve problems which are both cell degradation by read disturbance and power dissipation. Lowering 10% of the read voltage results in improving about 100 times of disturbance and decreasing 15% of power consumption. This scheme can also be helpful to nonvolatile memory using resistive cell such as MRAM, PRAM, and so on.

***Keywords*—** ReRAM; RRAM; Voltage Control; Read margin; Read disturb; ADC-based Sense Amp; power reduction

I. INTRODUCTION

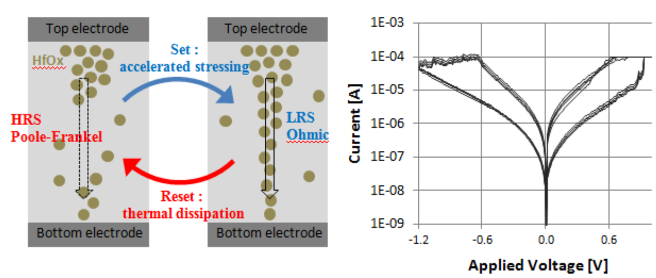
RESISTIVE random access memory (ReRAM) has been considered one of the promising candidates for next generation nonvolatile memory due to its superior scalability, simple structure, and high–speed switching operation. However, the cell resistance of ReRAM has wide distribution and is susceptible to the read/write disturbance, aging , and so on. To guarantee read reliability, many circuit designers have been studying about the ways to get optimum read margin to control reference current by analysis of resistance variations.

We focused on the ways to utilize this maximized read margin. This paper proposes a method to adjust the read voltage on read margin by read margin estimation based cell variation analysis using ADC. This method can lower read disturbance and reduce power consumption with little sensing speed degradation.

II. ANALYSIS OF CELL RESISTANCE VARIANCE

Resistive memory store the data using conductivity of cell. The cell conductivity can change high resistance state (HRS) or low resistance state (LRS) depending on bias condition across both ends. Generally, The ReRAM uses current mode sense amplifier to read cell data because of some benefit. So, the memory can read the data by comparing the difference between cell current and referent current for read operation. It is important to determine an appropriate reference current to get the optimum read margin.

The exact mechanism for the transition of ReRAM cell resistance is not clear yet and have been studied, since many physical and chemical basis such as Poole-Frenkel emission, Schottky emission, FN tunneling, Direct tunneling and traps tunneling are needed to explain it. Fig. 1(a) shows the expected mechanism of the transition between HRS and LRS. Depending on the voltage applied to both ends, the cell transition into set state by stress acceleration. And the Reset state can be changed by thermal dissipation. This operation is fully analog. So resistive memory has wide cell distribution. Fig. 1(b) shows the I-V curves for cell from measured data. The average set and reset voltage are 1.0V and -1.2V, respectively. Cell resistance can be changed by read disturbance. The read disturbance means that the cell states of set or reset are weakened due to stress of biasing or reading repeatedly. It can cause serious problem for reliable sensing data stored in cell because it can degrade the state of cell.



(a) (b)

Fig. 1 (a) Expected mechanism of HfOx-based ReRAM cell and (b) I-V curves from measured data

As one of the methods to overcome this problem, adaptive reference control(ARC) has been proposed to find the optimum read margin to control optimal reference current by using ADC (Analog – Digital Converter) to analyze cell distribution. In other words the cell resistance variation of analog information is converted digital code by ADC and the optimum read margin can be obtained by adjusting reference current with this digitalized cell distribution.[1] The concept of ARC to maximize read margin is showed in Fig. 2. Analyzing the set and reset current in each 50 and 50 samples, the reference current code is shifted to find optimum read margin and to keep the balance of read margin at each states from this sampling data.

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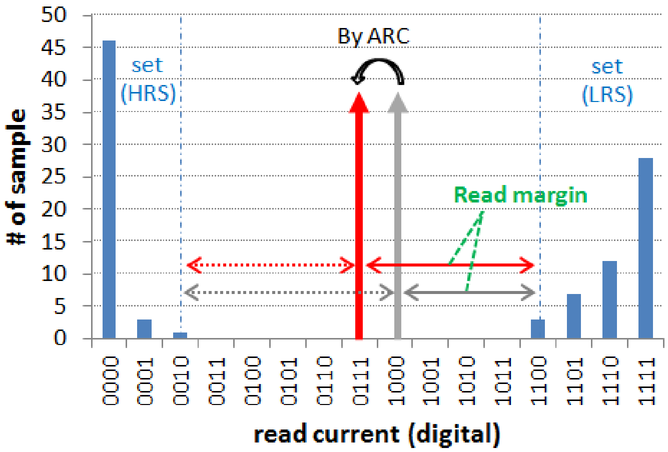
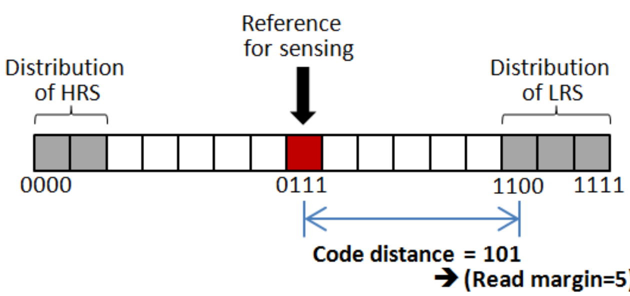


Fig. 2 Measured distributions of cell current and concept of Adaptive Reference Control (ARC)

III. Estimation of Read Margin

We find the optimum read margin by the analysis of cell variation and the adjustment of reference current. We could also find digitalized read margin. The code distance, the gap between reference code and min or max of cell variation code we analyzed will be coded read margin as illustrated in Fig. 3.



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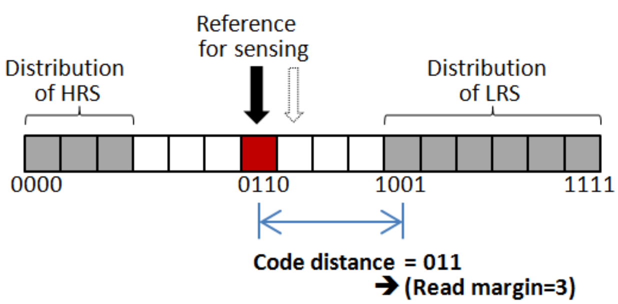

(b)

Fig. 3 the concept of coded read margin in cases of (a)narrow distribution and (b)wide distribution

The figure presents the coded read margin of memories with narrow distribution in Fig. 3(a) and wide distribution in Fig. 3(b). Fig. 3(a) shows case that has the distribution of HRS from '0000' to '0001' and the distribution of LRS '1100' to '1111' after analyzing read current by ADC. According to this information, the reference current is shifted from '1000' to '0111' to obtain the optimum read margin. Then the read margin become '101' as the gap between '1100' of the worst LRS and '0111' of reference current. In case of wide distribution can be understood similarly as shown in Fig. 3(b).

Fig. 4 shows the simulation result that if the delta current (we may call it read margin as analog information) which is the gap between reference current and cell current is higher than certain level, the gain in terms of speed is a negligible quantity. Using this margin, we intend to take the advantages of both read disturbance and power consumption by controlling the read voltage on the basis of code read margin.

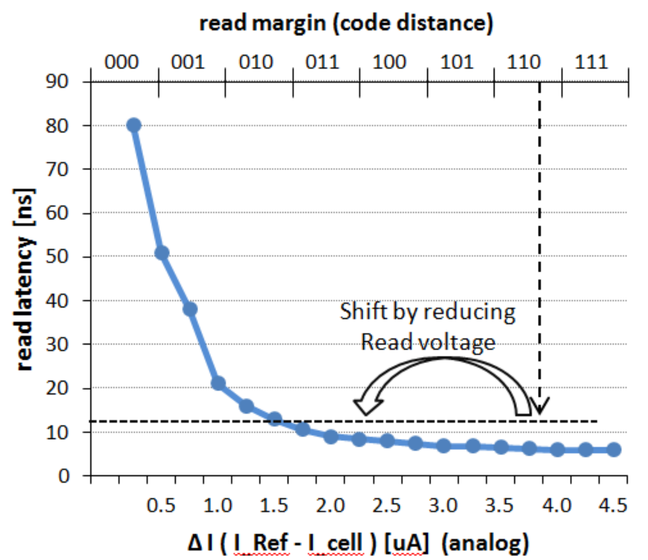

Fig. 4 Read latency of Sense-Amplifier as a function of read margin, or code distance in ADC outputs

IV. Adaptive Read Voltage Control

We obtain the maximized read margin by analysis of cell distributions and control of reference current. If we have enough read margin to sense valid data, we don't have to apply high read (sensing) voltage as shown in Fig. 4 .

In case of tight read margin (ex. Less than '011' in Fig.4), we have to apply a suitable read voltage to guarantee a accurate sensing data. But if we have enough read margin to sense , we can lower read voltage without the loss of sensing speed. Despite the read margin is large enough to sense , using relatively high sensing voltage will accelerate cell degradation by read disturbance because of high read current. The read voltage effect not only power dissipation but also read disturbance. We can improve cell disturbance with efficient power consumption by applying adaptive read voltage.

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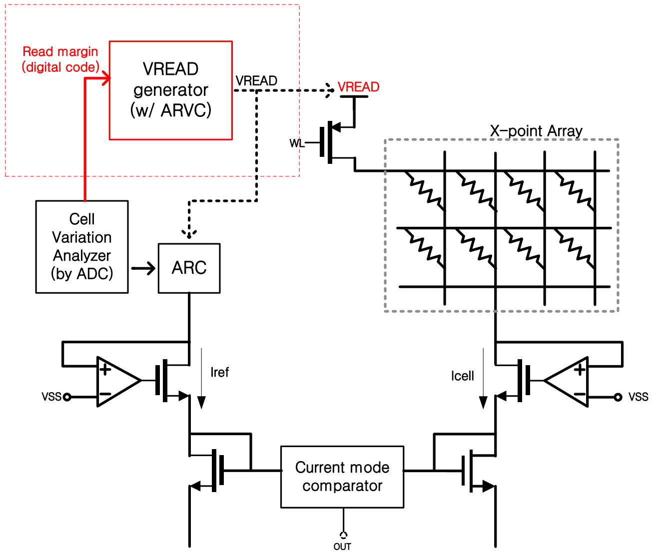

Fig. 5 The circuit diagram of adaptive read voltage control(ARVC)

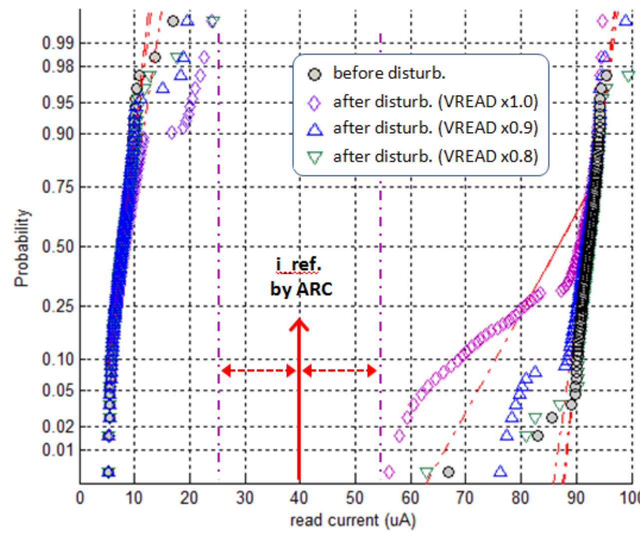

Fig. 7 The distribution of read current before and after 10^6 times of read disturbance at difference read voltage.

The simple circuit diagram of adaptive read voltage control (ARVC) for cross-point ReRAM is illustrated in Fig. 5. It consists of "Cell Distribution Analyzer(CDA)" analyzing the resistance distribution of cells by ADC from sampled cell or dummy cell for analysis and "Adaptive Reference Control(ARC)" adjusting reference current to maximize read margin. And we proposes to add read voltage generator with "Adaptive Read Voltage Control(ARVC)" adjusting appropriate read voltage on read margin to improve the read disturbance and consume power efficiently.

Fig. 7 shows the change of cell distribution by read disturbance in terms of read voltage. The graph demonstrates that when read voltage gets lower, the change of cell distribution by read disturbance is sharply reduced. It means that if possible, using a low read voltage is helpful to maintain a high read margin relatively. Conversely using a high read voltage accelerates cell degradation by read disturbance and this reduces the read margin. Finally it results in getting worse of reliability to read cell data.

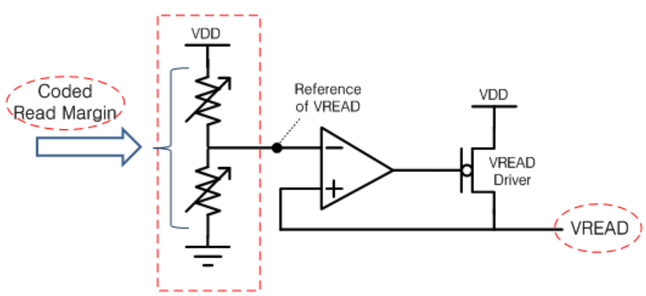

Fig. 6 The circuit diagram of read voltage generator with ARVC

Fig. 6 shows the simple circuit diagram of read voltage generator with ARVC. It is composed of the voltage divider that adjusts proper reference of read voltage(VREAD) by adjusting the resistance from coded read margin , OP-AMP that controls the strength of VREAD driver and VREAD driver. The reference level of VREAD is changed by coded read margin in accordance with predetermined design table on the basis of theoretical and experimental data. The VREAD is generated by this reference level in internal power generator.

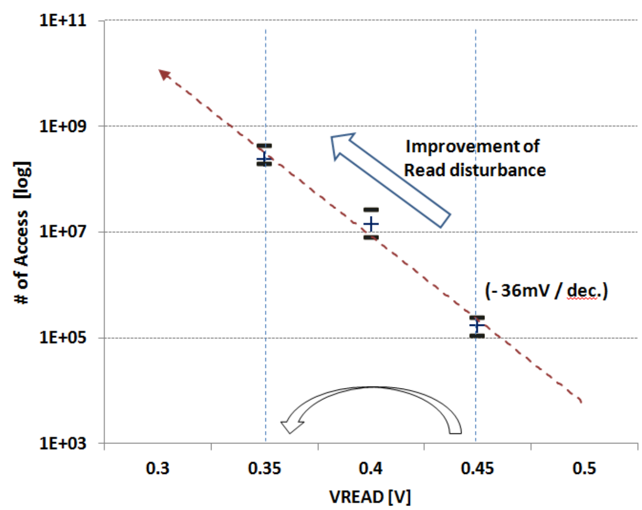

Fig. 8 Measured access-count-to-fail at different read voltage to estimate the sensitivity of disturbance

Fig. 8 is a graph of measured result that shows the improvement in read disturbance when lowering the read voltage from VREAD1(0.45V) to VREAD2(0.35V). We measured the number of access that the read margin falls below the target level by stressing consistently at different read voltage. The graph demonstrates that if read voltage is shrinking, cell degradation by read disturbance is reduced exponentially. The

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trend line of graph presents that the sensitivity is 36mV/dec. It means that lowering about 36mV of VREAD improves about 10 times of cell degradation by read disturbance as shown in Fig. 8.

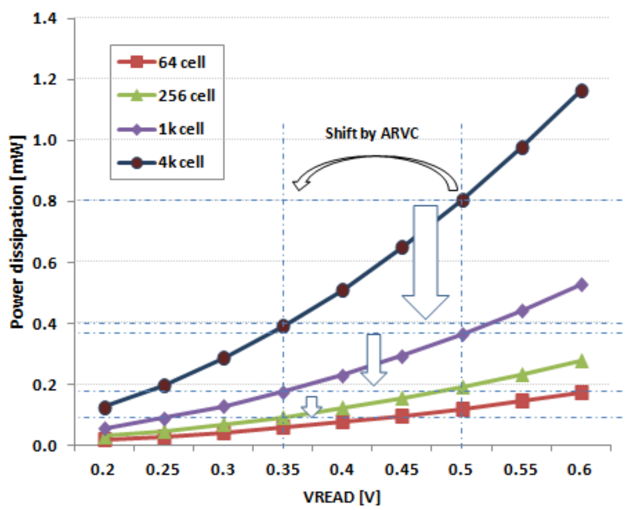

Fig. 9 Power dissipation of the read voltage change in various ReRAM density (simulation result)

Also Fig. 9 shows that read voltage and power consumption has great relationship. The graph demonstrates that in larger the density of memory array, the effect of power dissipation reduction by lowering read voltage gets greater. Because the sneak current is involved.

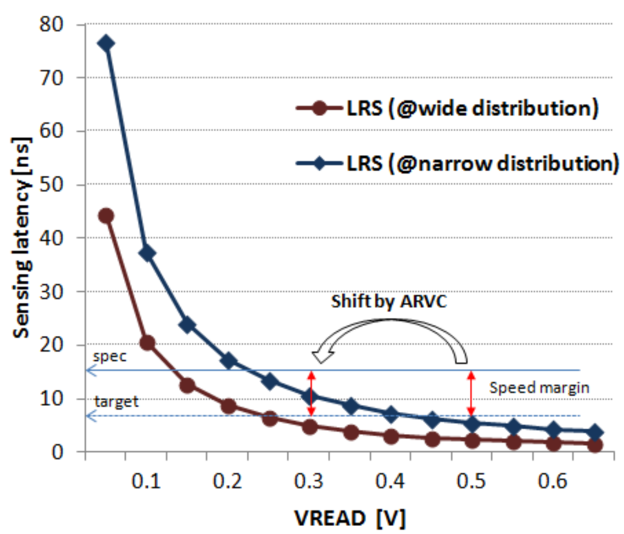

Fig. 10 sensing speed of the read voltage change (simulation result)

Fig. 10 shows the simulation result about sensing speed by changing read voltage. The graph presents that when the read margin exceeds a certain value, loss of sensing speed by lowering read voltage can be ignored. In other words, if we have a enough read margin to sense the accurate cell data, we can take advantages of read disturbance and power consumption by lowering read voltage without big loss of sensing speed.

V. Conclusion

We proposes an adaptive read voltage control (ARVC) that changes voltage control is effective reducing power dissipation and lowering read disturbance with same performance defined worst sensing speed. We simulated that Lowering read voltage 10% result in reducing 15% of power consumption and lowering about 100 times of read disturbance. Because of cell degradation by read disturbance, ReRAM may need to perform not only the hidden refresh by itself but also forced refresh by system if necessary. In this case, additional power dissipation increases and system performance is also degraded. The ARVC is necessary because this loss is serious in larger the array size of memory.

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Cascade nonlinear control of a continuous stirred tank reactor

Petr Dostál, Vladimír Bobál, and Jiří Vojtěšek

Abstract**—**The paper presents the cascade nonlinear control design of a continuous stirred chemical reactor. The control is performed in primary and secondary control-loops where the primary controlled output of the reactor is a concentration of the main reaction product and the secondary output is the reactant temperature. A common control input is the coolant flow rate. The controller in the primary control-loop is a P-controller with an adjustable gain The controller in the secondary control-loop is a controller consisting of the static nonlinear and the dynamic adaptive linear part. The proposed method is verified by control simulations.

Keywords**—**chemical reactor, cascade control, nonlinear control, external linear model, adaptive control

I. Introduction

The cascade control belongs to more complex control structures useful for such processes where more output variables can be measured and where only one input variable is available to the control. Principles of the cascade control are described e.g. in [1], [2] and [3].

Chemical reactors are typical processes suitable for a use of the cascade control. In cases of non-isothermal reactions, concentrations of the reaction products mostly depend on the temperature of reactant. Further, it is known that while the reactant temperature can be measured almost continuously, concentrations are usually measured in longer time intervals. Then, the application of the cascade control method can lead to good results. In this paper, the procedure for the cascade control design of a continuous stirred tank chemical reactor is presented.

Continuous stirred tank reactors (CSTRs) are units frequently used in chemical industry. From the system theory point of view, CSTRs belong to the class of nonlinear systems. Their mathematical models are described by sets of nonlinear differential equations (ODEs). The methods of CSTRs modelling and simulation can be found e.g. in [4] and [5].

In this paper, the CSTR control strategy is based on the fact that concentrations of components of reactions taking place in the reactor depend on the reactant temperature. Then, the main product concentration is considered as the primary controlled variable, and, the reactant temperature as the secondary controlled variable. The coolant flow rate represents a common control input. The primary controller determining the set point for the secondary (inner) control-loop is a P-controller with an adjustable gain. For the secondary controller, the procedure based on its factorization on linear and nonlinear parts is used. Basic ideas of this method can be found e.g. in [6] – [8]. The nonlinear static part (NSP) is obtained from simulated or measured steady-state characteristic of the CSTR, its polynomial or exponential approximation, and, subsequently, its differentiation. On behalf of development of the linear dynamic part (LDP), the NSP including the nonlinear model of the CSTR is approximated by a CT external linear model (ELM). For the CT ELM parameter estimation, the direct estimation in terms of filtered variables is used, see e.g. [9] – [11]. The method is based on filtration of continuous-time input and output signals where the filtered variables have in the s-domain the same properties as their non-filtered counterparts. The resulting CT controller is derived on the basis of the pole placement method, see, e.g. [12] or [13]. The control is tested by simulations of nonlinear model of the CSTR with a consecutive exothermic reaction.

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II. Nonlinear Model of the CSTR

Consider a CSTR with the first order consecutive exothermic reaction according to the scheme $A \xrightarrow{k_1} B \xrightarrow{k_2} C$ and with a perfectly mixed cooling jacket. Using the usual simplifications, the model of the CSTR is described by four nonlinear differential equations

$$\frac{dc_A}{dt} = -\left(\frac{q_r}{V_r} + k_1\right)c_A + \frac{q_r}{V_r}c_{Af} \tag{1}$$

$$\frac{dc_B}{dt} = -\left(\frac{q_r}{V_r} + k_2\right)c_B + k_1 c_A + \frac{q_r}{V_r}c_{Bf} \tag{2}$$

$$\frac{dT_r}{dt} = \frac{h_r}{(\rho c_p)_r} + \frac{q_r}{V_r}(T_{rf} - T_r) + \frac{A_h U}{V_r(\rho c_p)_r}(T_c - T_r) \tag{3}$$

$$\frac{dT_c}{dt} = \frac{q_c}{V_c}(T_{cf} - T_c) + \frac{A_h U}{V_c(\rho c_p)_c}(T_r - T_c) \tag{4}$$

with initial conditions $c_A(0) = c_A^s$, $c_B(0) = c_B^s$, $T_r(0) = T_r^s$ and $T_c(0) = T_c^s$. Here, t stands for the time, c for concentrations, T for temperatures, V for volumes, ρ for densities, c_p for specific heat capacities, q for volumetric flow rates, A_h is the heat exchange surface area and U is the heat transfer coefficient. Subscripts denoted r describe the reactant mixture, c the coolant, f the inlet values and the superscript s steady-state values.

The reaction rates and the reaction heat are expressed as

$$k_j = k_{0j}\exp\left(\frac{-E_j}{RT_r}\right),\ j = 1, 2 \tag{5}$$

$$h_r = h_1 k_1 c_A + h_2 k_2 c_B \tag{6}$$

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where k_0 are pre-exponential factors, E are activation energies and h are reaction enthalpies. The values of parameters, feed values and steady-state values are given in Table 1.

TABLE I
PARAMETERS, INLET VALUES AND INITIAL CONDITIONS

V_r = 1.2 m^3 V_c = 0.64 m^3 ρ_r = 985 kg m^{-3} ρ_c = 998 kg m^{-3}	c_{pr} = 4.05 kJ kg^{-1}K^{-1} c_{pc} = 4.18 kJ kg^{-1}K^{-1} A_h = 5.5 m^2 U = 43.5 kJ m^{-2}min^{-1}K^{-1}
k_{10} = 5.616 · 10^{16} min^{-1} k_{20} = 1.128 · 10^{18} min^{-1} h_1 = 4.8 · 10^4 kJ kmol^{-1}	E_1/R = 13477 K E_2/R = 15290 K h_2 = 2.2 · 10^4 kJ kmol^{-1}
c_{Af}^s = 2.85 kmol m^{-3} T_{rf}^s = 323 K	c_{Bf}^s = 0 kmol m^{-3} T_{cf}^s = 293 K
q_r^s = 0.08 m^{3}min^{-1}	

The desired reaction product is a concentration of the component B.

III. THE CONTROL SYSTEM DESIGN

A basic scheme of the cascade control is in Fig. 1.

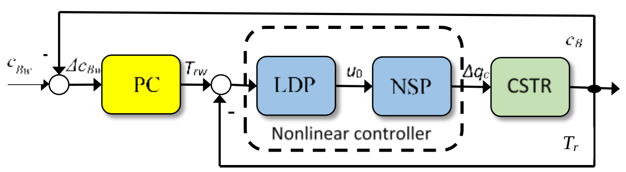

Fig. 1 Cascade nonlinear control scheme.

Here, PC stands for the primary proportional controller, LDP for the linear part and NSP for the nonlinear part of the secondary controller and CSTR for the reactor.

The control objective is to achieve a concentration of the component B as the primary controlled output near to its maximum. A dependence of the concentration of B on the reactant temperature is in Fig. 2.

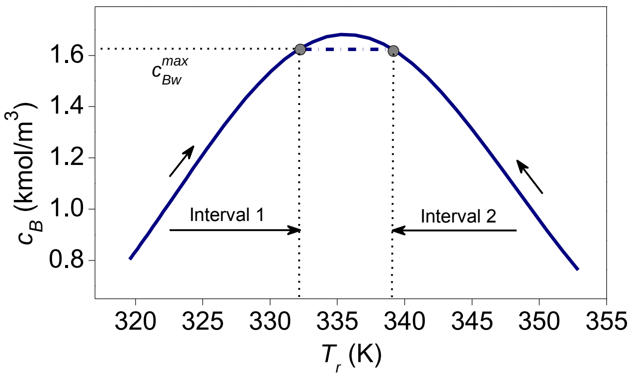

Fig. 2 Steady-state dependence of the product B concentration on the reactant temperature.

There, an operating area consists of two intervals. In the first interval, the concentration B increases with increasing reactant temperature, in the second interval it again decreases. Both intervals are limited by the maximum value $c_B^{\max} = 1.62$ kmol/m^2. It can be seen that the maximum value of c_B can be slightly higher then $c_B^{\max}$. However, with respect to some following procedures, the maximum desired value of c_B will be limited just by $c_B^{\max}$.

IV. THE PRIMARY CONTROLLER

The primary P-controller controller realizes the relation between the deviation of desired and actual c_b concentration and the corresponding desired reaction temperature according to the equation

$$\Delta T_{rw} = G_w \Delta c_{Bw} \tag{7}$$

Where G_w is an adjustable gain.

V. THE SECONDARY CONTROLLER DESIG

As previously introduced, the secondary controller consist of a nonlinear static and an adaptive linear dynamic part. The LDP creates a linear dynamic relation $u_0(t) = \Delta T_w(t)$ which represents a difference of the reactant temperature adequate to its desired value. Then, the NSP generates a static nonlinear relation betveen u_0 and a corresponding increment (decrement) of the coolant flow rate.

A. Nonlinear static part

The NSP derivation appears from a simulated or measured steady-state characteristics. The dependence of the reactant temperature on the coolant flow rate is shown in Fig.3. Both intervals are in accordance with intervals in Fig.2.

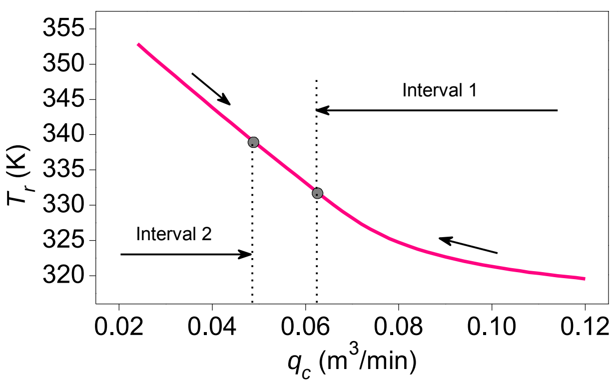

Fig. 3 Dependence of the reactant temperature on the coolant flow rate in the steady-state.

For purposes of later procedures, the boundaries of both intervals are determined as

$$0.12 \ge q_c \ge 0.062, \; 319.58 \le T_r \le 332.12$$

in the first operating interval, and,

$$0.049 \ge q_c \ge 0.024, \; 339.1 \le T_r \le 352.9$$

in the second operating interval.

With respect to required approximations, both coordinates are transformed as

$$\theta = \frac{q_c - q_c^{\min}}{q_c^{\max} - q_c^{\min}}, \quad \theta \in <0,1> \tag{8}$$

$$\psi = \frac{T_r - T_r^{\min}}{T_r^{\max} - T_r^{\min}}, \quad \psi \in <0,1> \tag{9}$$

where

$q_c^{\min} = 0.024$, $q_c^{\max} = 0.12$, $T_r^{\min} = 319.58$, $T_r^{\max} = 352.9$.

Then, transformed characteristics in both intervals are

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approximated as

$$\psi = -0.028 + 2.1336\exp(-\theta / 0.2383) \tag{10}$$

In the first interval, and,

$$\psi = 0.9965 - 1.6017\theta \tag{11}$$

in the second interval. The characteristics in both intervals together with their approximations are shown in Figs.4 and 5.

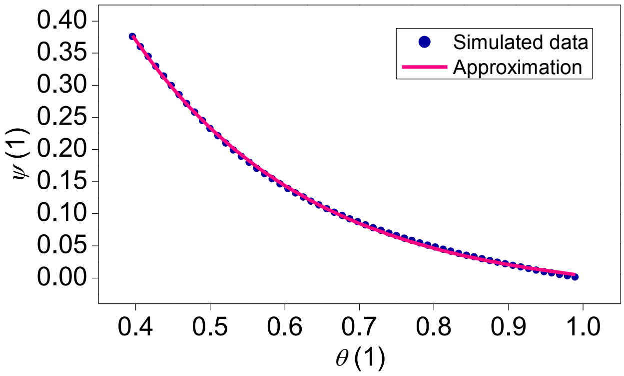

Fig. 4 Transformed steady state-characteristics in interval 1with approximation.

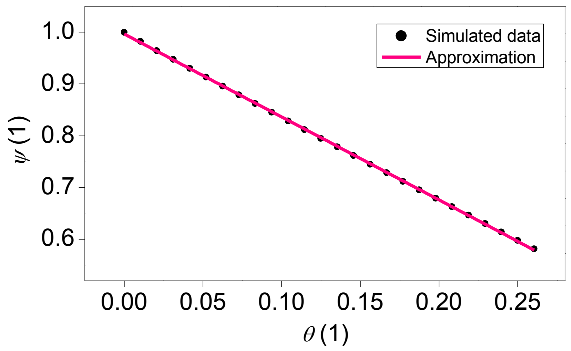

Fig. 5 Transformed steady state-characteristics in interval 2 with approximation.

Derivatives of expressions (10) and (11) needed to determine the function of the NSP are

$$\frac{d\psi}{d\theta} = -8.9534\exp(-\frac{\theta}{0.2383}) \tag{12}$$

in the first interval, and,

$$\frac{d\psi}{d\theta} = -1.6017 \tag{13}$$

in the second interval.

The relation between input and output of the NPC can now be formulated as

$$\Delta q_c = \frac{q_c^{\max} - q_c^{\min}}{T_r^{\max} - T_r^{\min}} \left(1 / \frac{d\psi}{d\theta} \right)_{\psi(T_r)} u_0 \tag{14}$$

where u_0 is the output of the LDP and $\psi(T_r)$ je a value of ψ according to T_r on the output of the CSTR.

B. CT external linear model of nonlinear elements

The nonlinear component of the closed-loop consisting of the NSP of the controller and the CSTR nonlinear model is approximated by a continuous-time external linear model (CT ELM) according to Fig. 6.

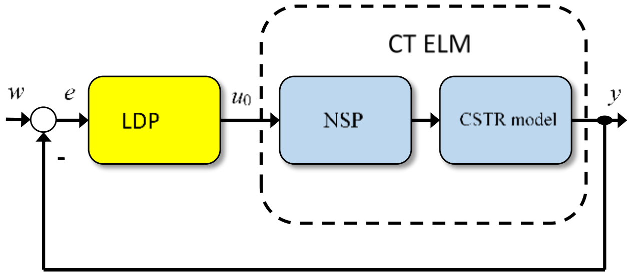

Fig. 6 Control system with CT external linear model.

where $w = \Delta T_{rw}$ and $y = T_r - T_r^s$.

It is well known that in adaptive control the controlled process of a higher order can be approximated by a linear model of a lower order with varying parameters. Here, the second order CT ELM has been chosen in the form of the second order linear differential equation

$$\ddot{y}(t) + a_1\dot{y}(t) + a_0 y(t) = b_0 u_0(t) \tag{15}$$

and, in the complex domain, as the transfer function

$$G(s) = \frac{Y(s)}{U_0(s)} = \frac{b_0}{s^2 + a_1 s + a_0} \tag{16}$$

C. CT ELM parameter estimation

The method of the direct CT ELM parameter estimation can be briefly carried out as follows.

Since the derivatives of both input and output cannot be directly measured, filtered variables u_f and y_f are established as the outputs of filters

$$c(\sigma)u_f(t) = u(t) \tag{17}$$

$$c(\sigma)y_f(t) = y(t) \tag{18}$$

where $\sigma = d/dt$ is the derivative operator, $c(\sigma)$ is a stable polynomial in σ that fulfills the condition $\deg c(\sigma) \geq \deg a(\sigma)$.

Note that the time constants of filters must be smaller than the time constants of the process. Since the latter are unknown at the beginning of the estimation procedure, it is necessary to make the filter time constants, selected a priori, sufficiently small.

With regard to (16), the polynomial a takes the concrete form $a(\sigma) = \sigma^2 + a_1\sigma + a_0$, and, the polynomial c can be chosen as $c(\sigma) = \sigma^2 + c_1\sigma + c_0$. Subsequently, the values of the filtered variables can be computed during the control by a solution of (17) and (18) using some standard integration method.

It can be easily proved that the transfer behavior among filtered and among nonfiltered variables are equivalent. Using the L-transform of (17) and (18), the expressions

$$c(s)U_f(s) = U(s) + \mu_1(s) \tag{19}$$

$$c(s)Y_f(s) = Y(s) + \mu_2(s) \tag{20}$$

can be obtained with μ_1 and μ_2 as polynomials of initial conditions. Substituting (19) and (20) into (16), and, after some manipulations, the relation between transforms of the filtered input and output takes the form

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$$Y_f(s) = \frac{b(s)}{a(s)} U_f(s) + M(s) = G(s) U_f(s) + M(s) \tag{21}$$

where $M(s)$ is a rational function as the transform of any function $\mu(t)$ which expresses an influence of initial conditions of filtered variables.

Now, the filtered variables including their derivatives can be sampled from filters (19) and (20) in discrete time intervals $t_k = k\ T_S$, $k = 0,1,2, ...$ where T_S is the sampling period. Denoting deg $a = n$ and deg $b = m$, the regression vector is defined as

$$\begin{aligned}\boldsymbol{\Phi}(t_k) = \big[&-y_f(t_k) - y_f^{(1)}(t_k) \ldots - y_f^{(n-1)}(t_k) \\ &u_f(t_k)\, u_f^{(1)}(t_k) \ldots u_f^{(m)}(t_k)\ \ 1\big]\end{aligned} \tag{22}$$

Then, the vector of parameters

$$\boldsymbol{\Theta}^T(t_k) = [a_0\ a_1\ ...\ a_{n-1}\ b_0\ b_1 ...\ b_m] \tag{23}$$

can be estimated from the ARX model

$$y_f^{(n)}(t_k) = \boldsymbol{\Theta}^T(t_k)\boldsymbol{\Phi}(t_k) + \mu(t_k) \tag{24}$$

Here, the recursive identification method with exponential and directional forgetting was used according to [14].

D. Linear Dynamic Part

For the adaptive control purposes, the 2DOF controller is used. It is known that this type of the controller often provides smoother control actions then a standard feedback controller. The 2DOF controller consist of the feedback part Q and the feedforward part R as shown in Fig. 7.

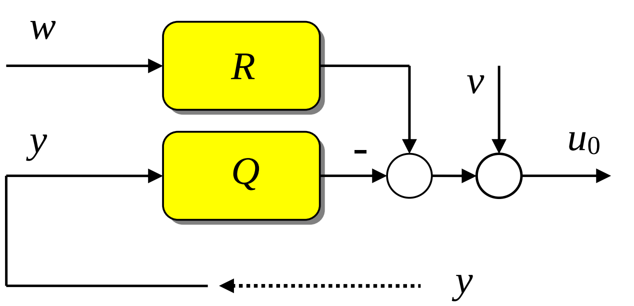

Fig. 7 The 2DOF controller.

In the scheme, w is the reference signal, y is the controlled output and u_0 the controller output. The reference w is taken into account as a sequence of step functions with transforms

$$W_k(s) = \frac{w_{k0}}{s} \tag{25}$$

In this paper, the disturbance is not considered.

The transfer functions of both controller parts are in forms

$$R(s) = \frac{r(s)}{p(s)}, \quad Q(s) = \frac{q(s)}{p(s)} \tag{26}$$

where q, r and p are coprime polynomials in s fulfilling the condition of properness $\deg r \le \deg p$ and $\deg q \le \deg p$. For a step disturbance with the transform (28), the polynomial p takes the form $p(s) = s\tilde{p}(s)$.

Using the polynomial theory, the controller results from a couple of polynomial equations

$$a(s)s\tilde{p}(s) + b(s)q(s) = d(s) \tag{27}$$

$$t(s)s + b(s)r(s) = d(s) \tag{28}$$

with a stable polynomial d on their right sides.

For the transfer function (16) with deg a = 2, the controller transfer functions take forms

$$\begin{aligned} Q(s) &= \frac{q(s)}{s\,\tilde{p}(s)} = \frac{q_2 s^2 + q_1 s + q_0}{s(s+p_0)} \\ R(s) &= \frac{r(s)}{s\,\tilde{p}(s)} = \frac{r_0}{s(s+p_0)} \end{aligned} \tag{29}$$

Moreover, the equality $r_0 = q_0$ can easily be obtained.

The controller parameters then follow from solutions of polynomial equations (27) and (28) and depend upon coefficients of the polynomial d.

In this paper, the polynomial d with roots determining the closed-loop poles is chosen as

$$d(s) = n(s)(s+\alpha)^2 \tag{30}$$

where n is a stable polynomial obtained by spectral factorization

$$a^*(s)a(s) = n^*(s)n(s) \tag{31}$$

and α is the selectable parameter that can usually be chosen by way of simulation experiments. Note that a choice of d in the form (30) provides the control of a good quality for aperiodic controlled processes. The polynomial n has the form

$$n(s) = s^2 + n_1 s + n_0$$

with coefficients

$$n_0 = \sqrt{a_0^2}\ , \quad n_1 = \sqrt{a_1^2 + 2n_0 - 2a_0}\ . \tag{32}$$

The controller parameters can be obtained from solution of the matrix equation

$$\begin{pmatrix} 1 & 0 & 0 & 0 \\ a_1 & b_0 & 0 & 0 \\ a_0 & 0 & b_0 & 0 \\ 0 & 0 & 0 & b_0 \end{pmatrix} \cdot \begin{pmatrix} p_0 \\ q_2 \\ q_1 \\ q_0 \end{pmatrix} = \begin{pmatrix} d_3 - a_1 \\ d_2 - a_0 \\ d_1 \\ d_0 \end{pmatrix} \tag{33}$$

where

$$\begin{aligned} d_3 &= n_1 + 2\alpha,\ d_2 = 2\alpha n_1 + n_0 + \alpha^2 \\ d_1 &= 2\alpha n_0 + \alpha^2 n_1,\ d_0 = \alpha^2 n_0 \end{aligned}. \tag{34}$$

Evidently, the controller parameters can be adjusted by the selectable parameter α.

VI. Simulation Results

All simulations were performed on nonlinear model of the CSTR. Considering the measurement of the concentration c_B in periods τ_s (min), the aim of simulations is to show an effect of this period and an effect of the adjustable gain of the P-controller G_w on some control responses. At the start of simulations, the P controller with a small gain was used. For the direct recursive parameter estimation, the sampling period T_S = 1 min was chosen. The value of the selectable parameter α is stated under each figure.

In this paper, only simulations in the first operating interval were performed. All simulations started from the point $c_B^s = 1.2$ kmol/m^3 and $q_c^s = 0.08$ m^3/min. The desired value of c_B has been chosen as $c_{Bw} = 1.6$ kmol/m^3 Effect of the

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parameter G_w on the reference w, the reactant temperature T_r and the concentration c_B responses is evident from Figs. 8, 9 and 10.

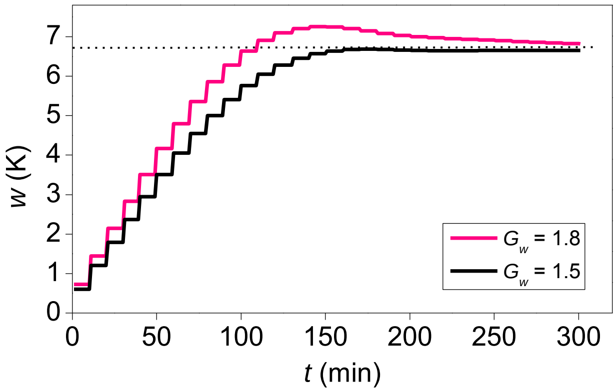

Fig. 8 Reference signal courses (τ_s = 10, α = 0.2).

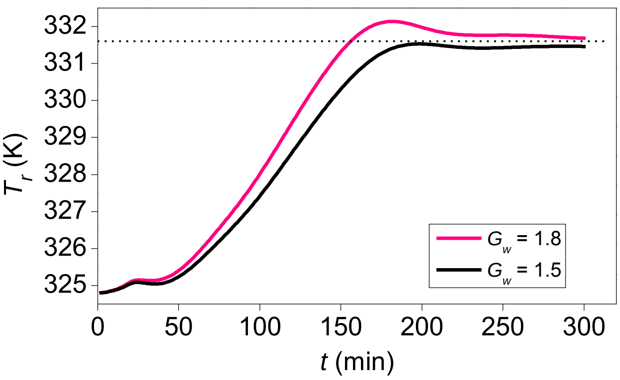

Fig. 9 Reactant temperature responses (τ_s = 10, α = 0.2).

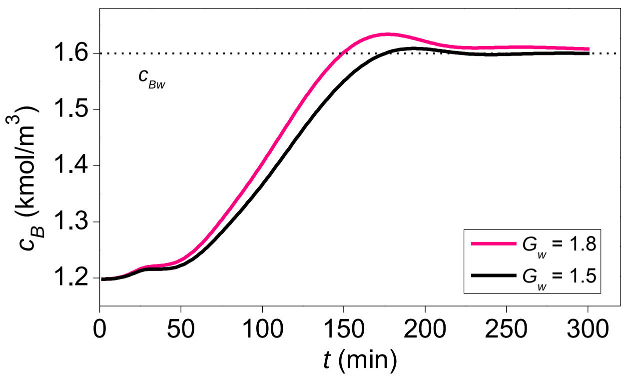

Fig. 10 Concentration c_B responses (τ_s = 10, α = 0.2).

It can be seen that an increasing G_w accelerates both signals in the control loop. However, its value is not unrestricted and its convenient value should be found experimentally. Strong sensitivity of the period τs on all responses can be seen in Figs.11, 12 and 13. Its shortening leads to significant overshoots. These, however, can be suppressed by setting a lower gain G_w. It should be to realize that τs is determined by possibilities of measurement.

Of interest, the coolant flow courses during control and under the same conditions can be seen in Fig. 14.

The adaptive controller parameters depend upon the selection of the parameter α. An effect of this parameter on the control quality has been in detail presented in other publications, see, e.g. [13].

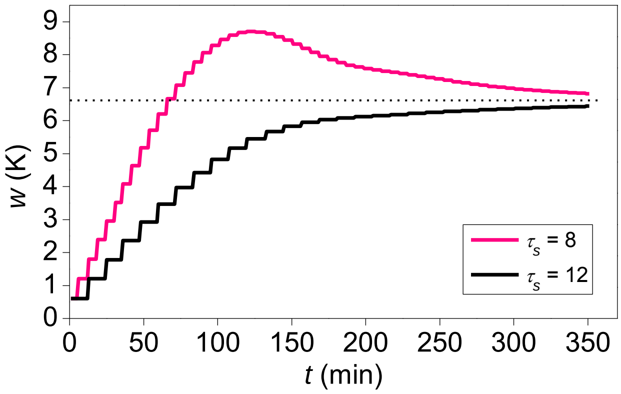

Fig. 11 Reference signal courses (G_w = 1.5, α = 0.2).

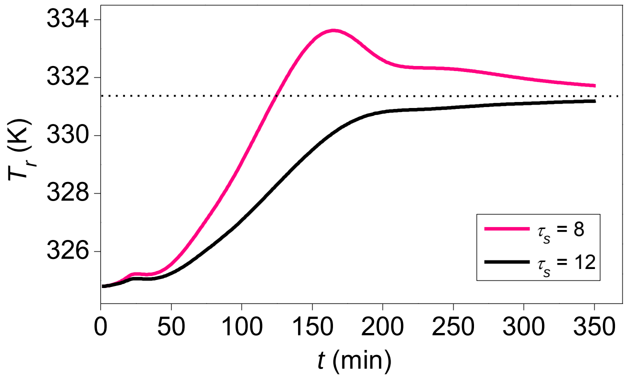

Fig. 12 Reactant temperature responses (G_w = 1.5, α = 0.2).

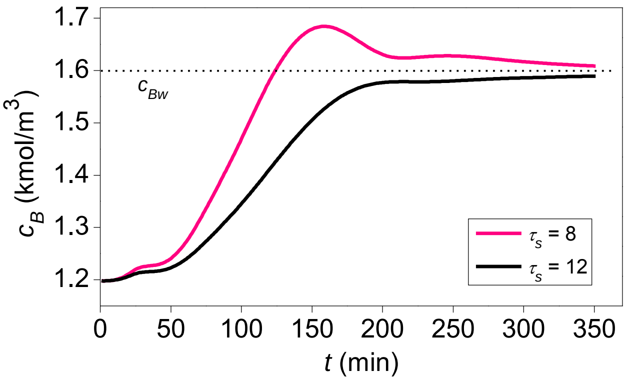

Fig. 13 Concentration c_B responses (G_w = 1.5, α = 0.2).

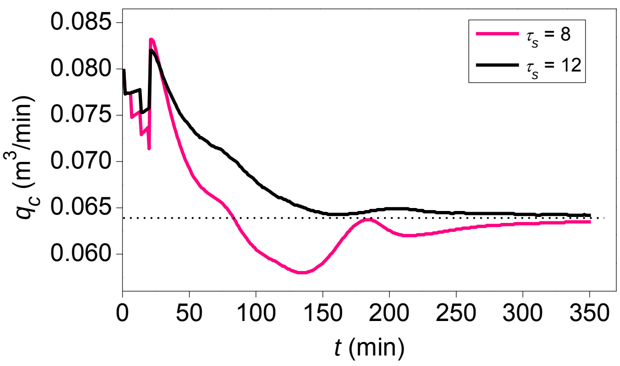

Fig. 14 Coolant flow rate courses (G_w = 1.5, α = 0.2).

VII. Conclusions

The paper deals with the cascade nonlinear control of a continuous stirred tank reactor. The control is performed in the external (primary) and inner (secondary) closed-loop where the concentration of a main product is the primary and the reactant temperature the secondary controlled variable. A common control input is the coolant flow rate.

The controller in the external control-loop is a P-controller with an adjustable gain. The controller in the inner control-loop is a nonlinear controller consisting of a nonlinear static part and an adaptive linear dynamic part in the 2DOF structure.For its derivation, the recursive parameter estimation, the polynomial approach and the pole placement method were applied.

The control was tested by simulations on the nonlinear model of the CSTR.

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Circuitry Design for Small Energy Harvest System

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Abstract**—**A circuitry design for energy harvesting purpose is investigated in this article. In particular, very low-power output harvested from the materials such as piezoelectric ceramics or polymer will be the focus of circuitry design for power management. Three-mode power management control including the fundamental supply, charge and supply, and hybrid converters is designed for the whole range of power output. The hybrid converter can combine the very low harvested power with a supporting battery so as to achieve a desired voltage for the load. A control circuitry by means of multiple comparators as voltage detectors and PWM generators is developed to control the switches and modes for the converters. Experiment testing is carried out to verify the function and efficiency of running individual mode at different input voltage respectively.

Keywords**—***Energy harvesting, Hybrid converter, Power management.*

I. Introduction

Sustainable energy technology attracts a lot of attention for the researchers to explore any possible solution and enhance its efficiency. No matter what resources such as solar or wind from ambient environment to harvest energy, converter and power management system plays very important roles. Different from many energy harvesting research works on large and heavy system, very low-power output is the target of building a suitable power management circuitry. Piezoelectric material, for example, is selected as the harvester with a smaller scale of mechanical vibration to electric energy conversion. Due to the low-power generation, how to design a converter that costs minimum energy in operation and is able to convert the rest of the harvesting energy into electricity is demanding and is the focus in this study. Piezoelectric materials are seeing more and more market ready applications thus getting more attention than before. Used as sensors, they are already one of the fastest growing technologies at present. However, as renewable energy sources, they are not as popular compared to the mainstream sources like wind and solar energy. This is mainly due to the low-power outputs of the piezoelectric materials. It has one advantage though, which is that it is very versatile, it can be created in various shapes, sizes at different mechanical designs. They are also versatile enough to be applied in other fields of renewable energy harvesting as its inherent ability of transforming mechanical vibrations to electrical energy is packaged in a small and compact size. With this, researches have been developed to create mechanical designs for the material. However, the circuitry to harvest and harness the power from it is as crucial. Since piezoelectric materials can only provide small power output, they are usually used stacked to each other just to create enough energy for driving small loads. Another inherent characteristic of these materials is that since they transform vibrations, not constant force, to electric energy, the resulting power output is in AC form. Therefore, it cannot be simply connected to a load; it has to be optimized as a DC power source. The waveforms taken from the piezoelectric materials are rarely perfect sinusoids, they have high-voltage spikes but quickly return to low power oscillations. This creates a challenge to create a circuit that will harness these various values of power at all times. Another problem is that with these vibrating power sources, stacking multiple pieces is not as seamless for the reason that if they are not in phase, one source might end up cancelling another source's output.

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II. System Configuration and Design Concept

This research tries to provide a complete power management solution to harvesting energy from a renewable energy source while simultaneously providing power to a load. This power management circuitry has been designed with piezoelectric materials in mind so the constraints and assumptions were derived from this particular field of energy harvest. The first constraint is that piezoelectric materials, compared to more mainstream sources like wind and solar energy, have very small output power mainly due to extremely small current values. This however, gives the researcher a bit more room to design the system with the voltage values. The second constraint is that piezoelectric materials generate power from the movement of its crystals; thus, the output power will be in AC form. The proposed design will be able to work with AC or DC forms of power input. With varying power outputs from the input energy source, the system should be able to provide the best management of power. The proposed design detects the voltage value from the energy source then automatically decides how the power will be harvested from the input and delivered to the load. There will be three modes of operation: Supply Mode, Charge and Supply Mode, and Hybrid Mode. If the energy from the source is enough to power the load, it will simply be modified to a desired output voltage value for the load's consumption. This will be done through a boost converter which is called the Supply Converter. This mode, which operates if the input voltage is at least 1.5 Volts, will be called the Supply Mode. At this time period, the battery is not affected in any way

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by the energy source and the load. The second case happens when the energy source can power the load and has enough power to simultaneously supply its energy to another branch. This happens if the input voltage is at least 2.5 Volts; again, this value is arbitrarily chosen for the purpose of this research. The energy that can still be distributed will be used to charge the battery. However, it has to be enhanced to a specific value to charge the battery by the use of another boost converter; this will be called the Charge Converter. In this time period, the energy source provides both for the load and the battery, this mode will be called Charge and Supply Mode. The third case is when the power from the energy source, even with the help of the Supply Converter, is not enough to reach the desired voltage for the load. In this situation, a special converter called the Hybrid Converter will be used to combine the power from the energy source and the battery to create the desired power output. This mode will be called the Hybrid Mode. Three mode converter diagram as shown in Fig. 1.

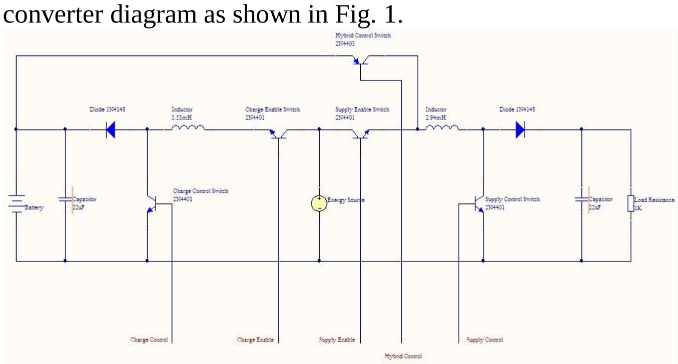

Fig. 1. Three mode converter

With this system design, there are five switches to activate and control the different converters and their duty cycles. Table 1 shows the corresponding inputs for different modes for the five switch controls.

Mode	*Charge Control*	*Charge Enable*	*Supply Enable*	*Supply Control*	*Hybrid Control*
Hybrid	OFF	OFF	Hybrid PWM	Hybrid PWM	Hybrid PWM
Supply	OFF	OFF	ON	Supply PWM	ON
Charge and Supply	Charge PWM	ON	ON	Supply PWM	ON

Table 1. Controller Inputs

To make the system able to decide for itself which mode should run at a specific time interval and provide the necessary PWM signals to switches, a control circuitry is proposed here. The Charge Converter is discussed apart from the Hybrid and the Supply Converters because it is basically stand-alone. It can work if it is connected with the other two converters or not. The Hybrid and Supply Converters, on the other hand, will be discussed together as they are now combined into one system to minimize the component count. The control circuit will utilize the following voltage sources for its decisions and PWM creation: Energy Source, Battery, Sawtooth Waveform at 100 kHz with voltages from 0 to 1.5V, VCC+ at 12V and VCC- at -5V. The operational amplifier chosen to serve as comparators is the AD843, which can operate at high-speed to accommodate the 100 kHz sampling rate of the whole system. Fig. 2 shows the control circuitry for the Charge Converter. The converter has two switches: the Charge Enable Switch and the Charge Control Switch. The control circuitry uses two comparators, Charge Comparator#1 and Charge Comparator#2 for the two switches, respectively. Their outputs are separated from the base of the transistors with 100 Ohm resistors to ensure the stability of the signal by allowing a small voltage separation with the base and the output of the operational amplifier.

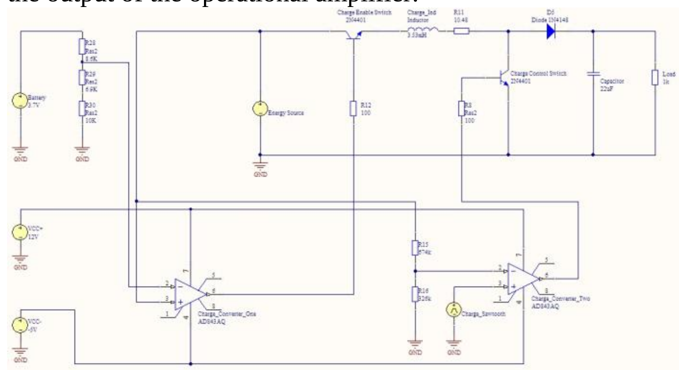

Fig. 2. Charge Converter with Control Circuit

Charge Comparator#1 serves detects if the system should run be in Charge and Supply Mode. A voltage divider circuit is connected to the battery to produce the necessary threshold voltage value, this will then be compared to the value of the input voltage from energy source. If the energy source is at least 2.50V, Charge Comparator#1 will output a high value closing the Charge Enable Switch, thus enabling the Charge and Supply Mode. If the input voltage is lower than 2.50V, the Charge Enable Switch will be opened by the low output of the comparator. The Charge Comparator#2 creates the PWM for the Charge Control Switch. It does so by comparing an optimized value from input voltage with the constant sawtooth waveform. This optimization of the input voltage value before comparison is done by a voltage divider circuit. The required voltage to create a specific duty cycle for multiple values of input voltage is calculated first, and then the resistor values are derived accordingly. Since the relationship between the input voltage and duty cycle is indirect, the sawtooth waveform has to be connected to the non-inverting terminal of the comparator. The result is listed in Table 2.

Input Voltage	Target Charge Control Duty Cycle	Charge Control Duty Cycle	Output Voltage
2.50	0.4626	0.457	4.292
3.00	0.3495	0.348	4.288
3.50	0.2374	0.239	4.125

Table 2. Charge Converter with Duty Cycle and Output

Fig.3 shows the control circuit for the combined Supply and Hybrid Converter. It uses three operational amplifiers as comparators. Hybrid Comppparator#1 detects if the input voltage is lower than the threshold for Hybrid Mode. This threshold voltage is created by the voltage divider circuit connected to the battery, the same with the one connected with Charge Comparator#1 in the Charge Converter control circuit. Hybrid Comparator#1 outputs a high value if the Hybrid Mode will operate and a low value if the Supply Mode should be activated. This output will be an important control for the two other comparators.

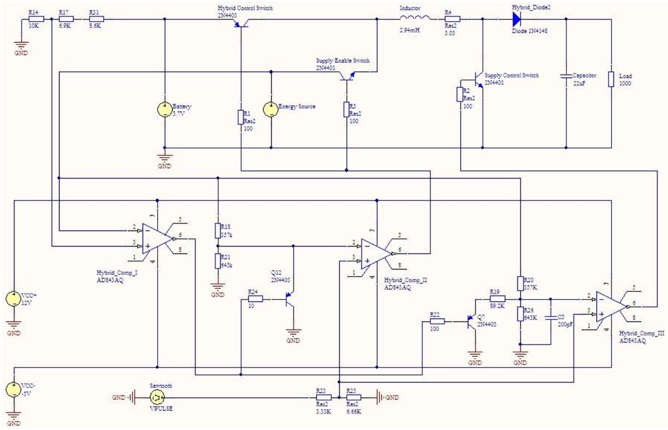

Fig. 3. Hybrid Converter with Control Circuit

Hybrid Comparator#2 outputs the control waveform for these two switches. If the system activates Hybrid Mode, Hybrid Comparator#1 outputs a high value thus, disabling transistor Q12; this will be an open switch. The input to the inverting terminal of Hybrid Comparator#2 will be a positive value, optimized by a voltage divider circuit from the input voltage, and will be compared to the sawtooth wave which itself is only two-thirds of the original value; peak voltage of 1.0V. This is done due to the design constraints of having small voltages from the energy source during Hybrid Mode. For the Hybrid Comparator#3, the input to its inverting terminal is controlled by a variably switched voltage divider. Since in Hybrid Mode, the output Hybrid Comparator#1 is high, transistor Q7 will be an open switch, thus the input the Hybrid Comparator#3 will be the same with the input to Hybrid Comparator#2. These two comparators will then have the same output, which is consistent with the desired PWM control signals from Table 1. If the input voltage is at least 1.5V, the system will work in Supply Mode; this combined converter will act as the Supply Converter. Since Hybrid Comparator#1 outputs a low value, transistor Q12 will be a closed switch, grounding the inverting terminal of Hybrid Comparator#2. Consequently, the sawtooth waveform will always be greater than inverting terminal input; this will create a constant high value output for Hybrid Comparator#2. This will allow the Supply Enable Switch to be closed and the Hybrid Control Switch to be opened. The low output of Hybrid Comparator#1 will also turn-on transistor Q7, this will change the resistor values of the voltage divider for optimizing the energy source voltage for the inverting input of Hybrid Comparator#3. The connected resistor value is calculated such that once connected in parallel with R26, the inverting terminal of Hybrid Comparator#3 will get exactly 18% of the input voltage. This value is pre-calculated to create the necessary voltage for comparison with the sawtooth wave and produce the PWM waveform for the Supply Control Switch during Supply Mode.

Input Voltage	**Target Supply Control Duty Cycle**	**Supply Control Duty Cycle**	**Output Voltage**
0.50	0.6783	0.6785	6.097
0.75	0.5724	0.5178	5.939
1.00	0.4992	0.357	4.767
1.25	0.4404	0.1983	4.281
1.50	0.7327	0.7300	5.012
2.00	0.6395	0.6400	5.415
2.50	0.5476	0.5500	5.415
3.00	0.4563	0.4600	5.801
3.50	0.3655	0.3700	5.563

Table 3. Hybrid/Supply Converter with Duty Cycle and Output

Table 3 shows the target and produced duty cycles for the PWM signals. For this combined converter, the desired output voltage is constant at 5.0V. It can be seen that there is disconnect with the constant decrease of the target supply control duty cycle with increasing input voltage at 1.25V and 1.50V. This is due to the transition of the system from Hybrid Mode to Supply Mode which has their own PWM waveform requirements.

III. Experiment and Results

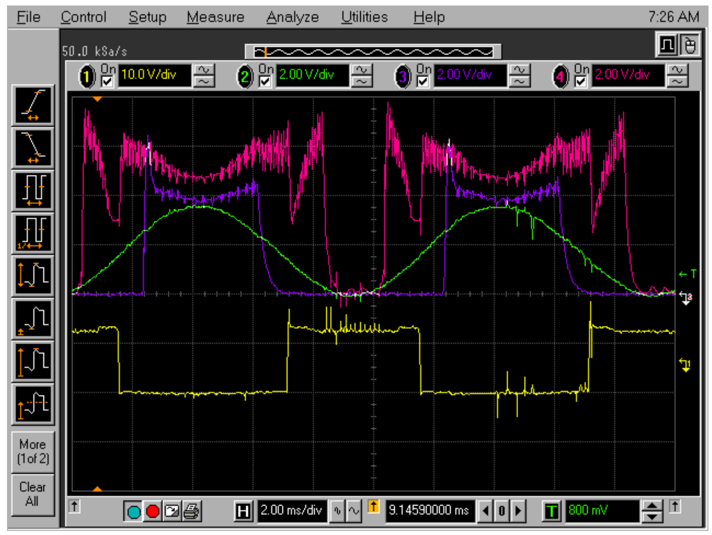

Fig. 4. Oscilloscope Waveforms with 100nF Output Capacitor

Fig. 4 shows the oscilloscope data from the experiment. The green wave is the input voltage, which is a 100Hz sine wave. The purple wave is the output of the Charge Converter; this will be connected to the battery to charge it during Charge Mode. As seen from the graph, it outputs a 4.0V when the input voltage is higher than 2.50V; this will be enough to charge the battery. The yellow wave is the Hybrid Indicator; it is the output of the first comparator in the control circuit for the Supply and Hybrid Converters. It will return a high value if the Hybrid Mode is running. This means that if the input voltage is lower than 1.50V, the Hybrid Indicator will be a high voltage value. However, if the input voltage is at least 1.50V, the Hybrid Indicator will be low. This wave is fluctuating between 6.0V and negative 6.0V. Finally, the pink wave shows the output of the Supply Converter and the Hybrid Converter, which is integrated, and will be connected to the load. In theory, it should be a constant 5.0V. As seen from the graph, when the Supply Mode is running, the output voltage is fluctuating around 5.0V; it is not very smooth because of the 100nF capacitor connected in parallel to the load. During Hybrid Mode, the circuit also aims for 5.0V, however, it is not a constant 5.0V volts either. This is consistent with the previous experiment data that there is nonlinearity in the relationship between the input voltage and the Hybrid Converter duty cycle and that to successfully produce a 5.0V in the output, the Hybrid Converter needs at least 0.50V from the input or energy source. As seen from the graph, once the input voltage

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drops below 0.50V, the output to the load also drops. However, it is a positive sign that even if the Hybrid Converter does not produce a smooth 5.0V output, it is able to produce an output voltage that is higher than the input voltage or the battery output. This proves that the Hybrid Mode design principle is working. By connecting a bigger capacitor to the load, the output voltage can become smooth and a steady 5.0V. As shown in Fig. 5, a 220uF capacitor was used instead of the 100nF used in Fig. 4. Fig. 4 will be useful in showing how the system really behaves because the capacitor does not create much smoothing. However, for applications, Fig. 5 is more useful for reference.

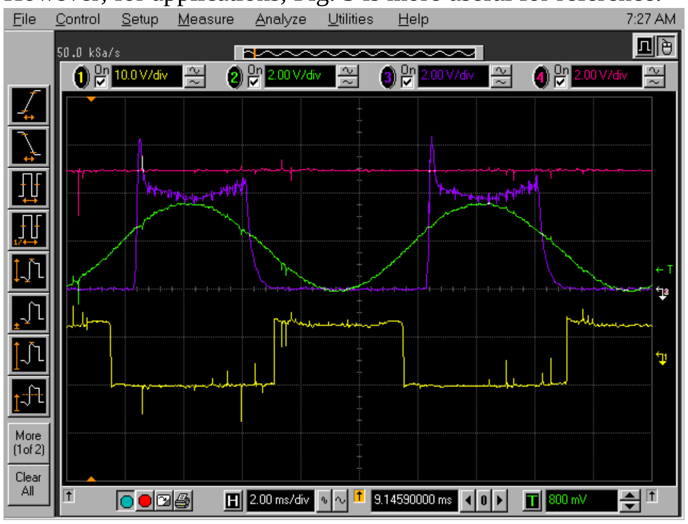

Fig. 5. Oscilloscope Waveforms with 200uF Output Capacitor

IV. CONCLUSION

The research proposed a newly designed Hybrid Converter as part of the three-mode power management circuit. The experiment data showed that at different voltage values from the piezoelectric, a different mode can and should be used to properly provide power to the load while keeping high operating efficiencies. Besides the tested effectiveness of the design, it also keeps the energy source and the battery grounded at all times. This is very important because with this, measuring the input voltage from energy source will be much more reliable as its value will be always being absolute to ground. With the battery grounded at all times, other parts of the circuitry can be connected to it. As shown in the proposed control system, the voltage divider for choosing the threshold voltages is connected to the battery without any effect to its voltage, and thus to its operation in the Hybrid Converter. The autonomous three-mode power management system is successfully built in the experiment. The desired mode ran in their thresholds voltages and the duty cycles are produced properly to control the boost converters. To make the output smoother, a larger capacitor can be used, both for the Supply/Hybrid Mode and the Charge Converter. This opens up the possibility of connecting multiple charging circuits and hybrid converters to it. The research can be extended to have multiple energy sources with their own converters and control circuits. This can be used in applications where the energy sources have low power values that one piece is not enough, like piezoelectric materials.

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An Adjustable HVDC Power Supply using Integrated High Voltage Transformer with Some Protective & Controlling Features.

Nader N. Barsoum, Muhammad Muktadir Rahman

Abstract— We can produce variable/adjustable HVDC with a little arrangement using Fly back Transformer (IHVT), Tesla coil, car ignition coil & other type of step-up auto transformer found in microwave oven, X-ray units & in similar devices. This arrangement of circuitry is very reliable & light weight. In our experiment we made a power supply using Integrated High Voltage Transformer & try to give it several protective & controlling features to its driver circuitry to increase the longevity of the power supply. As far as the general run of small-scale electronics is concerned, EHT (extra high tension)/HVDC power supplies are used mainly for cathode ray tube (CRT) anodes and for some specialized purposes such as Geiger-Muller counters and photomultipliers. None of these applications calls for a large current drain. As an example, X-ray equipment may require 100 kVDC at a current of less than 1 A. Some of these EHT supplies such as those used for radio transmitters or particle accelerators demand very substantial currents. As an example, large radio transmitters may call for a 20 kVDC supply at several amperes of current.

Keywords **—** Adjustable, HVDC, Spark gap

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I. Introduction

There is no precise definition of what is now meant by EHT (extra high tension)/HVDC, but the original idea was that valve operated equipment could normally be expected to use voltage levels up to 500 VDC and anything higher than this was EHT, whether for a valve transmitter circuit, a TV cathode ray tube, X-ray tube or high voltage test equipments. The typical Fly back Transformers (IHVT) used in TV sets are similar to those high frequency transformers which are used in SMPS supplies. Using these Fly back Transformers, one can build a HVDC supply. The circuit is known as *flyback power supply* (see Fig. 1) which is similar to SMPS supplies. EHT supplies for laboratory use require considerably better stabilization than those used for TV sets, but the general principles follow much the same lines as are used in SMPS supplies.

II. Experiments

We have implemented the circuit (Figure: 1) on bread board & PCB with necessary power supplies. Where Q_1 and Q_2 are driver and output transistors respectively. The output transistor is operated as an electronic switch, which when forward biased, saturates to close and on reverse biasing cuts-off to cause an open circuit. When in saturated mode, it has to deliver large bursts of power to the secondary coil of FBT.

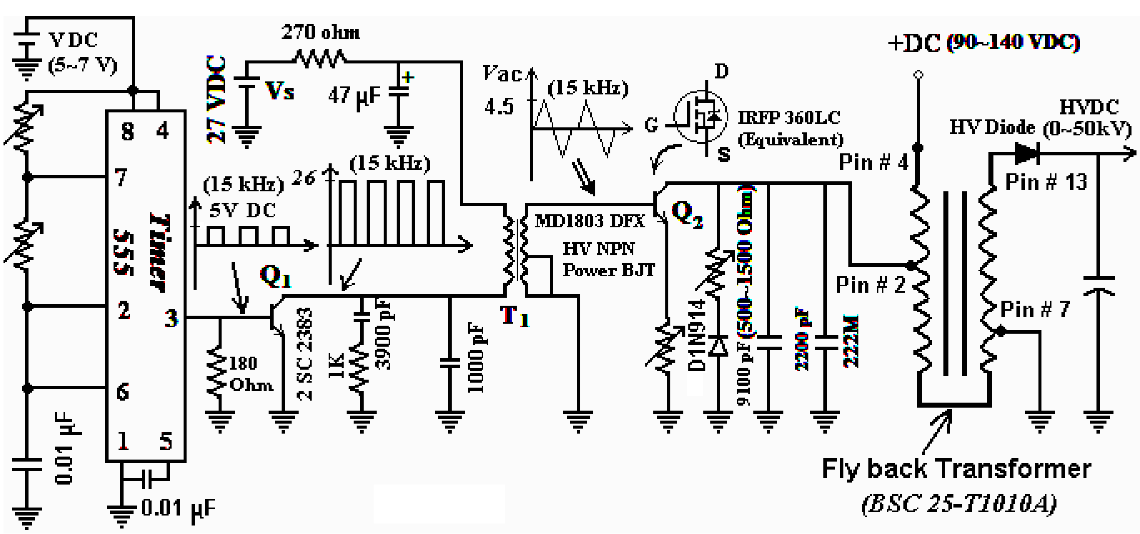

Figure: 1 Driver Circuit

Therefore, it is of great importance that the controlling voltage waveform fed to the base of Q_2 shall always be large enough to firmly turn it 'on' yet also sufficiently negative to reverse bias it when required to be cut-off. The transistor Q_1 is also operated as an electronic switch and triggered into conduction by positive pulses applied at its base. These pulses are received from the oscillator which is formed by 555 timer IC. When Q_1 is saturated its collector is nearly earthed and when turned-off, the collector voltage rises to about the same value as the supply voltage (V_s). Thus the waveform appearing at the collector of Q_1 takes the form of a series of square wave or rectangular pulses of amplitude nearly equal to V_s. These are fed at the base of Q_2 through coupling (step-down) transformer T_1 .The coupling transformer has a primary-to-secondary turns ratio of about 6:1 designed to match the high output impedance of Q_1 into the low impedance base circuit of Q_2. The high step-down turns ratio also ensures that a negative pulse of about 5V can be applied to the base of Q_2 when it is desired to turn it off. The connections of T_1 are so arranged that the 'turning-on' of Q_1 causes Q_2 to 'turn-off' and conversely. Output transistor, Q_2 is a class "C" amplifier. Basically the amplifier operates like a switch, operating at a frequency from 1 kHz to several kHz. It operates at either saturation or cutoff. Some of these supplies use a bipolar transistor, while others use a MOSFET power transistor to pulse dc current through the primary of the IHVT [1],[6].

III. Results and Observation

Flyback transformers cannot be connected to the mains directly. They start working at a frequency of about 1 kHz, whereas the mains have only 50Hz. The higher frequency has many advantages, such as smaller and lighter cores, smaller caps for rectifiers etc. We vary frequency of the square wave (received from the oscillator) from 1.5 kHz to 82.5 kHz (with a variable duty cycle from 48%-90%). If we increase frequency of the Oscillator then the arc (at the secondary side of Fly back transformer and the spark gap between EHT cord and ground lead is approximately 1cm which indicates a spark-over voltage with a peak of 30 kV in air at 20^0C and 760 torr pressure) [2] seems more thick with less whining which indicates an decrease in EHT/HVDC (Fig. 7). If we decrease frequency of the oscillator then the diameter of the arc will become thinner with a hissing sound which indicates an increase in EHT/HVDC (Fig. 2).

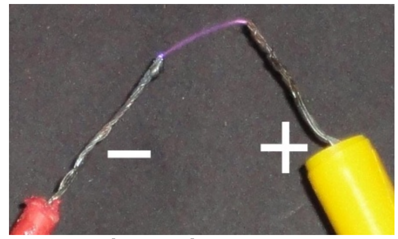

Figure: 2 Spark Gap indicating an increase in HVDC

Arc will not sustain if the frequency of the oscillator is less than 1.5 kHz. If we increase duty cycle (%) of the square wave (received from the oscillator) then the arc at the secondary side of FBT becomes thinner. If we decrease duty cycle (%) of the square wave of the oscillator then the arc at the secondary side of FBT seems very thick [9,10]. In our experiment when the duty cycle of the square wave of the oscillator is ≥ 98%, thin arc vanished suddenly. In addition to higher voltage requirements, some applications need more current and also some degree of stabilization. The current requirement is met by using larger currents in the primary of the coupling transformer (T_1) so that the amount of power that is switched through Q_2 is substantially higher. Output or driver transistors may have collector voltages as low as 26 volts, but they will draw up to 1.0 ampere or more current. Therefore, transformer windings, rectifiers, and filter chokes of necessary power supplies need to have higher current ratings [5]. If alternating sine wave has applied at the base of Q_1 then it will damage the power BJT (Q_2) as well as the oscillator but before that it works for a while (like few seconds). If E_S(secondary voltage) of FBT is increased, it causes an increase in I_P (primary current) and thus damages Q_2. Adding capacitors (912H, 222M) in parallel (Figure: 3) between collector & emitter/Drain & source of HV power BJT/ nMOS (Q_2) will decrease the voltage (EHT).

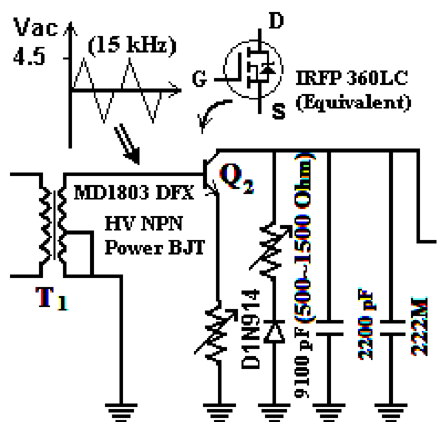

Figure: 3 Output Stage

We can increase HVDC by modifying the Fly back transformer primary winding by adding turns and extending the winding on the same core. Using voltage multipliers (triplers, generally), we

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can reduce the high-voltage requirements of the FBT by a large factor. Voltage tripler modules are used to obtain this additional high voltage. This arrangement also minimizes the insulation requirements of the FBT. In HVAC system (conventional power system) line/phase lead becomes hot whereas an opposite thing happens in case of HVDC. In HVDC supplies, ground lead becomes too hot and it melts down during running a load of high R (Fig. 7). Finally the overall results will be optimum if we use an oscillator which produces less noisy pulse (here square wave).

IV. PROTECTIVE & CONTROLLING FEATURES

Although there is an inbuilt damper diode in the power BJT/nMOS (Q_2), we have used an extra 2W diode (polarity inconsequential). The resistor in series with this diode can not have a value less than 500 Ω to avoid damage to the resistor. This is critical in limiting the magnitude of the peak value of the collector emitter voltage during excessive arcing. Thus protective features of the entire schematic shown in figure: 4 ultimately comes down to the D1N914 and its series resistance which clearly brings significant changes in EHT [6]. Increasing the value of R_e, we can make the Q_2 more sustainable.

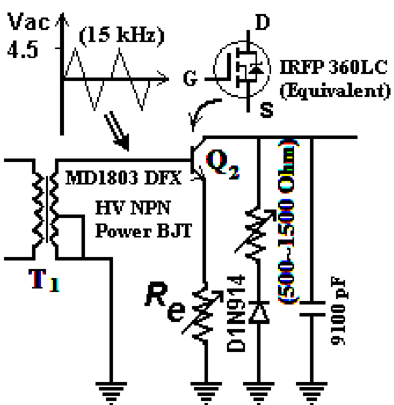

Figure: 4 Output Stage

Using power MOSFET as Q_2 one may achieve performance much superior to using bipolar power transistors. Since the best performance characteristics of the MOSFET come forth when the device is operated at very high frequencies (normally 100 KHz and above), certain design precautions must be taken in order to minimize problems, especially oscillations. There is one simple design rule associated with MOSFET application which will prevent the transistor from oscillating when used in high frequencies. First, minimize all lead lengths going to the MOSFET terminals, especially the gate lead. If short leads are not possible, then the designer may use a ferrite bead or a small-value resistor in series with the gate of the MOSEFT. Either one of those elements when placed close to the transistor gate will suppress parasitic oscillations. Another important thing to remember is the fact that the silicon oxide layer between the gate and source regions can be easily perforated and therefore permanently destroyed if the gate-to-source voltage exceeds manufacturer's specifications. Practical gate voltages have a maximum value anywhere from 20 to 30 V. Even if the gate voltage is below the maximum permissible value, it is advisable to perform a thorough investigation to make sure that there are not any fast rising spikes, caused by stray inductances, which may destroy the oxide layer of the MOSFET. Also it is very important to realize that in the case of inductive reactance/inductance, the ohmic opposition is proportional to the frequency. The frequency of the applied current has a very significant effect on the operation of magnetic components like transformers and inductors. The higher the frequency, the faster is the rate at which the current changes. For example, if the applied current had a frequency of 120 cycles per second instead of 60, the current flowing through the coil would change twice as fast. The faster the current changes, the faster the magnetic field about the inductor expands and collapses. Because the magnetic lines of force move so much faster, they induce a higher emf in the coil. In other words, the faster moving magnetic lines cause the coil to offer an even higher opposition to the flow of AC current and therefore the lower is the current flow through the single winding of the auto transformer which makes the very thin wire of the single winding of IHVT more sustainable. There are several advantages to designing converters working at, say, 100 KHz rather than 20 KHz, the most important being reduced size, weight and the acoustical noise. The power MOSFET offers the designer a high speed, high power, high voltage device with high gain, almost no storage time, no thermal runway and inhibited breakdown characteristics. We can add a distant controlling feature by replacing $R_a$and $R_b$with some light dependent resistor or photo conductive cell (Fig. 5). Then by controlling the intensity of the incident light to those photo resistive parts, we can control the driver circuitry (Fig.1). Finally we need to control the intensity of the incident light from a distance to achieve our goal.

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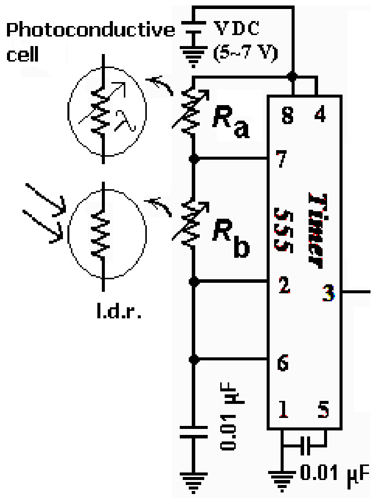

Figure: 5 Oscillator

V. MEASUREMENT & INSTRUMENTATION

It is not possible to check directly the voltage pulse waveform at the anode of the high voltage rectifier, because the peak-to-peak amplitude of the pulse may be as high as 50KV. It is possible, however to see the pulse on a scope by bringing the scope probe near the anode lead of the rectifier. There is enough capacitive coupling to give an indication. We have also used a HV probe (Fig.6), connected with a DMM to measure HVDC. A spark gap (Fig.7) can be used for measurement of the peak value of the HVDC [7]. Air is a poor conductor of electricity. However if two conductors are separated by a small gap of air /gas, it is possible to make the electric current jump across the gap. 1 cm spark gap in air between EHT cord (pin # 13) & ground lead (pin #7) indicates a spark over voltage of 30 KV (peak) approximately. If the arc gap becomes too long, the applied voltage could be insufficient to maintain the arc and it breaks off. A modern digital multimeter with functions of measuring actuating quantities like, frequency and duty cycle is adequate for this experiment.

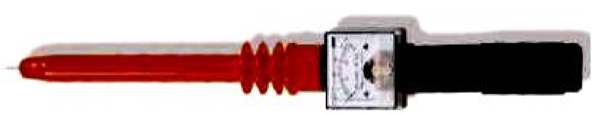

Figure: 6 HV Probe

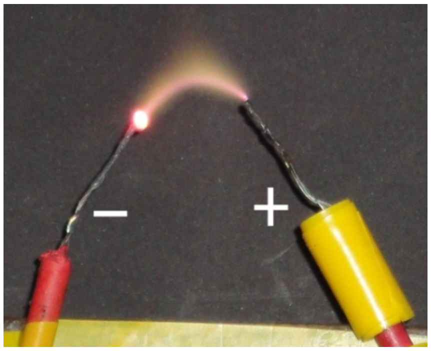

Figure: 7 Spark Gap indicating decrease in HVDC

VI. CONCLUSION

The circuit works and is great for many things, such as drawings arcs, Jacob's ladders, charging capacitors, running a HV cascade (not recommended for beginners!), powering plasma globes & lifter, and even powering a small Tesla Coil. Any work on EHT supplies should be carried out with great cautions, because capacitors in the circuit may have been charged to several kilovolts [3]. Even though EHT supplies may be current limited and capacitors values are small compared to the electrolytic capacitors that are used in low voltage supplies, the discharge of a capacitor can represent a large amount of energy which can prove fatal. Switching off and discharging capacitors may not be safe either, because some types of capacitors exhibit a form of voltage hysteresis, so that after being discharged they can build up voltage again and when work is to be carried out on an EHT supply, all capacitors should be discharged properly.

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Internet Traffic Trends and Major Security Challenges In Local &Internet Cloud

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ABSTRACT

With the immense development in the field of communication almost every business is partially dependent on internet. Cloud's computing popularity has changed the way in which companies and individuals can think to process the data and to store the information. This is a nice opportunity through which anybody can access any kind of data or applications and then while sitting at any part of the world. On the other hand this liberty is also the major cause in many of the security breaches; in this paper we discussed cloud computing architecture, different security issues in local and internet cloud.

Keywords: *Cloud computing, virtualization security, Community cloud, Authentication, Data security, Cloud security, Security as a service.*

1. INTRODUCTION

Cloud computing is an innovative computing model, which has originated with distributed computing, grid computing, parallel computing, utility computing, virtualization technology and many other technologies. It offers data storage, large-scale computation, virtualization, high expansibility and reliability at the same time low price service. Cloud computing has severe security issues that can badly affect its rapid development.

With increased popularity, organizations are facing some key security and privacy issues in adoption of this innovative model. It has been observed that the traditional protection mechanisms need reconsideration to be deployed for providing security to cloud computing architecture. Security of cloud computing is the main issue that is delaying its adoption by IT organizations

Cloud and its characteristics

Accessing any computer services without knowing computers physical condition or location is virtually known as cloud computing. There are other characteristics by which cloud can be distinguished. i.e. by on demand service a cloud use can one-sided get provision of using computing services, storage services, network services without going in detail and without human interaction to each service. Broad network access privilege is also available by the use of standard techniques of using heterogeneous network client include think or think client platforms. By the use of clouds companies shared their resources by resource pooling through which computing, broadband network, memory and storage resources are pooled and are available for different users for their heterogeneous nature of requirements without knowing details about physical location of these backend pooled resources. Capabilities can be automatically available to fulfilled the run-time or on demand services. To the consumer, the available capabilities are appeared as to be unlimited and can be approached at any time in quantity. Resources are automatically controlled and optimized by leveraging a metering capability1 at some level of abstraction which are appropriate for some services like processing storage, bandwidth and user accounts which also give a privilege to print report for resources usage by the use of histogram to ensure transparency for both consumer and service provider.

Figure 1: Basic Building Blocks for Cloud Computing

2. CLOUD SERVICE MODELS

Several models for cloud services are available a brief introduction about these models is given below.

2.1. Software as a Service (SaaS) is the feature that is available for users to use the applications, which are running on the cloud infrastructure of service providers with the provision to give access to clients by different client end applications or by the use of web-based clients. The good thing about this kind of services is that the consumer don't need to be worried about cloud infrastructure, its network, operating systems its storage or capabilities of application and their configuration.

2.2. Platform as a Service (PaaS) through this capability the consumer can enjoy the facility to deploy an application created by the consumer by using any programming its normally done by charge per use or pay per use basis. In general a cloud is an infrastructure, which is combination of hardware and software having five basic characteristics of cloud computing which can be viewed as a physical layer and abstraction layer. One end which is containing all the hardware resources is called the physical layer. All these hardware resources are responsible to complete computing, storage and network services while on the other hand the abstraction layer consisting of software deployment on the physical layer. The good thing is that the consumer don't manage the infrastructure instead he has the control on his deployed applications and even he can modify the configuration of the application.

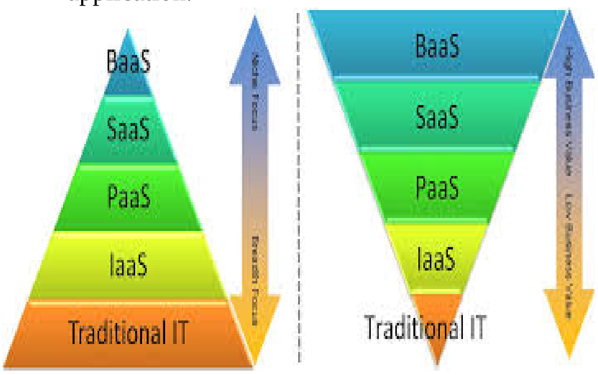

Figure 2: Clouds building blocks in hierarchy

2.3. ***Infrastructure as a Service (IaaS).*** Through this model the consumer have the liberty to access processing, networks, storage and many other fundamental resources to use them as platform for deployment of software and other applications. The consumer is not responsible for management of cloud infrastructure but still enjoy the liberty to manage the features and functions of operation system like selection of network firewall.

3. CLOUD DEPLOYMENT METHOD

Several types of clouds are avail based on the functionality and architecture we can classify them into following types.

3.1. ***Public cloud***. Offers an Infrastructure, which gives liberty of open use of this cloud by the general public. Its ownership and management might be by third party, some organization, government agency, some research institute or it might be joint venture of above entities.

3.2. ***Private cloud***. Offers an Infrastructure, which allows only exclusive use of this cloud by a single organization having multiple units, or outlets, which require data store and management. Its ownership and management might be by third party, some organization, government agency, some research institute or it might be joint venture of above entities.

3.3. ***Community cloud***. Offers an Infrastructure which allows only exclusive use of this cloud for exclusive use by any specific community having some specific concerns and consumer needs, services and information requirements which require data store and management. Its ownership and management might be by third party, some organization, government agency, some research institute or it might be joint venture of above entities.

3.4. ***Hybrid cloud***. Offers an Infrastructure which is actually a combination of two or more than two cloud (public, private or community) they remain unique entities and on the other hand they are bound by some standardized technology which allows the portability of application and data at the same time. i.e. for load balancing between the clouds we often use cloud bursting.

4. RELATED WORK

Tremendous work have been done by researchers in the field of cloud computing, its architecture, security and its services.

Pedro Costa et al described Despite the vast adoption of the Cloud concept, most Decision Makers (DM) in IT industry have expressed concerns and doubts about how, when and what should be migrated to the Cloud as there are no strict standards in adopting cloud Computing. So they stated their problem as "DM cannot evaluate Cloud services in IT organizations" and proposed a solution with a set of thirty measurement criteria evaluated on two cloud services; Google Apps and Microsoft Office 365. For evaluating their proposal they interviewed clients, suppliers and experts of cloud computing and calculated their point of views using Likert Scale. Figure 1 shows the graphical representation of the results on the set of criteria vs. likert scale. Analysis of the results found that criteria Availability, Confidentiality, Access Control, Reliability, and Data Privacy and Loss have vital role in Cloud services whereas criteria as Confidentiality, Risks, Flexibility, Supportability, Innovation, and Efficiency are essential for organizations too. However, least importance was credited to Accessibility, Auditability, Pricing Strategy, Provider Qualifications, and Accuracy. They conclude that Security and Performance are the key areas for which IT organizations are crucial about. [8]

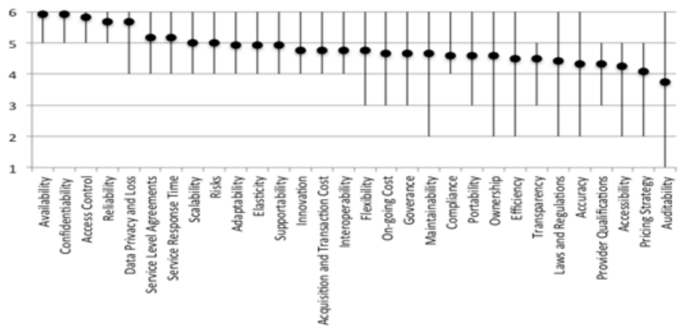

Figure 3: Thirty Measurement Criteria for cloud computing [8]

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As we can see from figure 3 shows Thirty Measurement Criteria for cloud computing calculated on a Likert Scale by Pedro costa et al [8]

Using Cloud computing, one may question when data or information has been transferred from on to off premises where there is no logical or physical control and probably unknown premises, what happens to it? Similarly, the location of the data is not provided by the cloud providers, so one doesn't know where data is stored. Hence we can say that the data doesn't remain physically secure. As an example, everyone is sharing resources in a public cloud, owned by the cloud providers, where they do not have any idea or control of where resources are located because the resources are in a shared pool, which is outside the control of organization. While information transfer, who will be responsible for encryption/decryption keys, either organization (customer) or the provider? These and many other questions still require researcher's attention [9].

Cloud Security issues have been categorized into Security and Privacy, Loss of Control and Data, Insider Threats, Outside Malicious Attacks, Interoperability, Multi-tenancy, and Costing Model

5. CLOUD COMPUTING SECURITY& PRIVACY ISSUES

Where cloud computing can help organizations accomplish more by paying less and breaking the physical boundaries between IT infrastructure and its users, here are few issues that need to be addressed.

a. Security & Privacy

As stated earlier, security has played a vital role in delaying the adoption of Cloud computing. Without any doubt, it appears daunting to many when putting ones data, installing ones software on someone else's hard disk by using someone else's Computer. Existing prominent security issues such as loss of data, phishing, botnet (working on a collection of machines remotely) create very serious threats to both data and software. Moreover, the cloud model with new characteristics such as multi-tenancy and the concept of pooled computing resources has introduced new security challenges that need new mechanisms to tackle with. For example, as Cloud has the ability to provide more reliable botnet infrastructure services at a cheaper price, hackers are now at an ease to start an attack. [10]

Similarly, organizations still feel alarmed for data privacy in moving their data on to the Cloud. Currently, there are two IT systems; IT management and personal applications that are considered easier to move on to the cloud. Organizations have fear in employing IaaS as compared to SaaS. The reason is that because insignificant functions are usually outsourced to the Cloud, and important functions are kept within on premise. According to a survey, in three years time, 31.5% of the organization will shift their Storage Capacity to the cloud. However 46.3% of organization's collaborative Applications will be moved to the cloud, which is relatively very high as compared to the storage capacity. [10]

b. Loss of Control and Data

Moving data and services on to Cloud has always been a daunting task for the organizations. This is due to the fact that they don't have information about the geographical storage of data as the cloud provider can host them anywhere within the cloud. When organizations port their data or services to cloud, they are not aware of the location of their data and service. The fear experienced by the organizations have grounds as they are totally unaware of any security mechanism for their vital data whether implemented or not by the cloud provider as the organizations have no control over their own data once ported on the cloud. The multi-tenancy property of the cloud is quite beneficial on one hand but at the same time can become dangerous. If proper security mechanism is not employed, it may allow access control to unauthorized parties to sensitive data. Therefore data loss and leakage can be disastrous to the organization's financial reputation and customer count loss. For example, records can be deleted or altered by hackers when moved to off premises where there is no proper security measures implemented. There are a lot of factors responsible for data loss such as unauthorized access, insufficient authentication and accounting control, conflicting use of encryption keys, operational breakdown, service disruption and unreliable data center. [9]

A possible solution to the stated problems is the use of strong network authentication, authorization processes and exchange the key is another method to ensure the security and which are known and transparent to the cloud customers and providers.

c. Insider Threats

Many of the times, it has been seen that an organization experiences threats within itself. In cloud environment, getting infected from this threat has even greater chances because of multi-tenant infrastructure, under the umbrella of provider's single management domain. Actually the organization lack transparency of processes adopted by cloud provider's for its implementation. The processes include hiring of new employees, locating data and making relationships with third party vendors. No visibility of hiring standards and practices for cloud employees is a great insider malicious threat as providing space for casual hacking corporate espionage. Without going through any security mechanism, a third party vendor for the provider can knock into the sensitive data and sell it to the organization's competitors. Hence, insider threats that are currently malfunctioning in small to very large-scale enterprises need special attention. [9]

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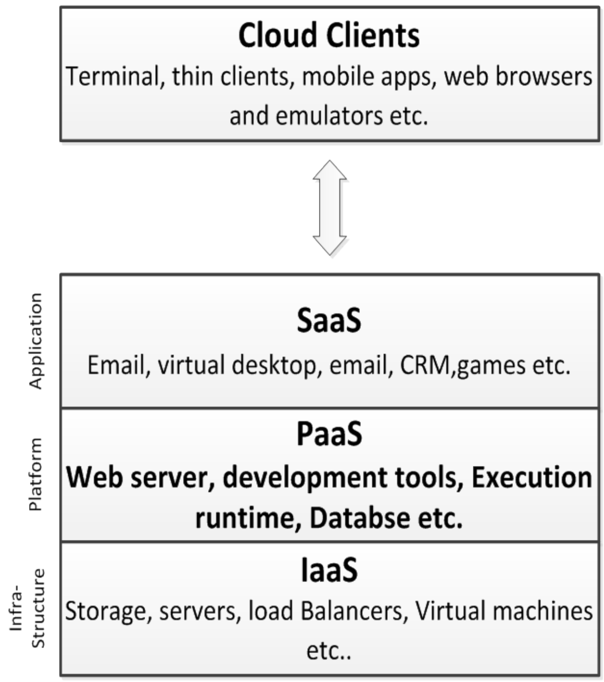

Figure 4: Layers in clouds

d. Outside Malicious Attacks

Clouds are designed to help its authorized users easily access information with more interfaces. Consequently with this infrastructure, outside threats come into existence and become one of the most alarming and persistent issues for any organization. These attacks results in discharge of confidential data in possible defacing of the organization. Hackers and attackers take the advantage by exploiting API limitation, breaking the media or logical connection or by using methods in social engineering. Although outside attacks may not be as harmful as inside attacks but they are difficult to cover up because the media intensify such attacks that can play an extremely destructive role in an organization’s reputation and credibility. [9]

e. Interoperability

The “Hazy Cloud” phenomenon suggests that each cloud offers specific criteria for its users, applications and providers to interact with the cloud. This obstructs the formation of cloud ecosystems by employing vendor locking, which does not allow users to select at the same time among other vendors/offering for optimizing resources at different levels on premises. Furthermore, clouds APIs are complex enough to integrate existing system of the organization withcloud services. The main objective of cloud interoperability is to recognize the flawless data flow within and between clouds and local applications. There are many reasons why interoperability is considered essential for cloud computing. Most importantly, organizations need to keep their core competencies and IT assets on premises while outsourcing insignificant functions like human resources on to the cloud. Secondly, for optimizing data and services, organizations may require to outsource services provided by other vendors that are usually least significant. Standardization is a good explanation for addressing interoperability issue. As cloud adoption has delayed, the interoperability problem has not disturbed industry cloud vendors much. [10]

f. Multi-tenancy

With the benefits like cost saving, data aggregation and release management offered by multi-tenancy environment, there are some critical problems associated with it in terms of security. Multiple users are sharing same software applications and physical hardware in a cloud, acting as tenants accessing same resources provided by the cloud provider. Therefore, data loss and information leakage are serious threats faced in this environment. [10]

As an example, there are businesses running in Europe that operates on strict data privacy laws monitored by government agencies. These laws state that data about French customers need to be located only inside France servers, German customer data inside Germany, etc. Therefore, cloud applications need to be implemented from different data centers in multiple countries across Europe. So it becomes a vital issue for cloud providers to make it happen. As another example, if a cloud provider has two or more organizations from the same industry, then for competitive reasons, each organization will never allow its secret idea to be located on the same physical server as data from its rival organization.

g. Costing Model

Adoption of cloud computing can significantly reduce the infrastructure cost; however data communication cost may experience an increase. For example, the initial cost of transferring an organization's data and services to and from public and community Cloud and the cost per unit of computing resources is probably higher. Regular data centers calculate their cost based on utilization of static computing whereas the in a cloud environment, elastic resource pool has complicated the cost analysis. Similarly, the cost analysis is performed by a virtual machine rather the underlying physical server. The cost of providing multi-tenancy includes re-designing and redeveloping the single-tenancy software. There is an immense increase in cost for providing new cloud features such as intensive customization, performance and security enhancement for simultaneous user access, and solving the problems introduced by developing these changes. It is therefore important for SaaS providers to consider the trade-off between implementation of multi-tenancy and the cost-effectiveness achieved through multi-tenancy such as compact number of on-site software licenses and reduced amortization overhead etc. For that reason, it is important to develop a strategic cost model for SaaS cloud providers for their sustainability and productivity. [10]

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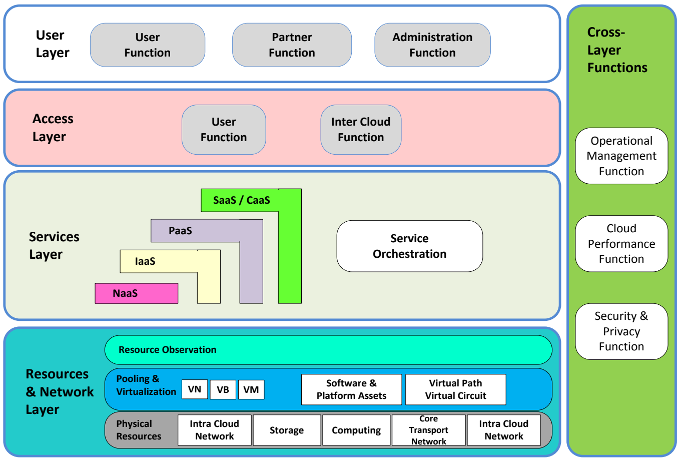

Figure 5: Functionality of Clouds at different layers

6. CONCLUSION

Conclusion always based on facts with supporting details of data so here we conclude our work on the basis of results of our findings with this note that cloud is the future of all the cutting-edge technologies and any resistance to ignore or avoiding cloud services will eventually go unsuccessful and no organization will be able to keep their data and business plans away from clouds in the long run as it the era of information technology but the smart way is to consider all these security issues and apply the suitable solution which help to stop breach of security of data.

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Design and Optimization of a 300 MSamples/s Track and Hold Architecture for a 5-bit Flash ADC in 180nm CMOS Technology

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***Abstract*—This paper introduces the design and optimization of a Track and Hold (T/H) architecture that find application at the front end of a fully differential 5-bit flash ADC (Analog to Digital Converter). To minimize non-linearity and charge injection the architecture relies on bootstrapping and bottom plate sampling. The circuit is implemented using a standard 180nm six-metal layer digital CMOS technology and it operates from a 1.8V supply. The sampling frequency achieved is 300 MSamples/s, which is consistent with the range of applications sought for the ADC. The design has been validated through simulation. The errors between analytical derivations and simulations are within 10%.**

Keywords—Track and Hold (TH); Analog to Digital Converter (ADC); CMOS Technology; Integrated Circuits.

I. INTRODUCTION

In many of today's high performance applications, including telecommunication and biolectronics systems, there is a common trend towards designs where an ADC interface is integrated with several complex digital signal-processing (DSP) blocks. By moving the ADC as close as possible to the front end of the chip, more DSP functionalities can be included, and therefore the system robustness, scalability and flexibility is increased [1]. Nevertheless, these benefits do not come for free and moving the ADC closer to the front-end imposes more stringent speed requirements. With MOSFETs feature sizes scaling down to nanometer dimensions and cutoff (f_T) and oscillation frequencies (f_{MAX}) of production processes in the hundreds of GHz, CMOS technology has become an attractive platform for implementing low cost, high-speed, and low power consumption ADCs [2]. Beside the CMOS technology's improvements, the other key enabler for achieving high-speed ADC systems is the application of time interleaving [3]. Time interleaving allows to increase the sampling rate of an ADC system by a factor of n, with n being the number of sub-ADC employed. ADCs with large interleaving factors can achieve sampling rates much higher than those of a single sub-ADC.

This paper presents the design of a 300MSamples/s track and hold (T/H) circuit used inside a 5-bit flash sub-ADC that is part of an eight-fold time-interleaved converter array. Track and hold circuits are one of the key blocks required for implementing high-speed analog-to-digital converters (ADC). Over the years a number of CMOS T/H circuits have been researched and developed [4][5]. The optimum choice for a T/H circuit is highly dependent on the application's requirements and the technology avaliable [6]. As a result, designing the best T/H circuit for a given application is an extremely difficult task and it constitues an on going research challenge.

The rest of the paper is organized as follows. Section II describes the typical operation and non-idealities that affect the performances of any MOS-based T/H circuit. Section III discusses the proposed T/H architecture and its benefits. Section IV illustrates the viability of the proposed architecture and it validates it through simulation. Finally, section V summarizes the results of our work and provides conclusions.

II. MOS-BASED TRACK AND HOLD

Fig.1 portrays the most basic structure of a T/H circuit. In its simplest form a T/H circuit consists of a MOS switch and a sample capacitor C_S. Ideally when the switch is ON, current charges the capacitor to the input voltage, and then when the switch is turned OFF, the resultant voltage is held on the capacitor. Unfortunately the MOS is not an ideal switch, so a number of non-idealities plague the performances of this "supposedely" simple structure. Fig.2 shows equivalent lumped models for the basic T/H circuit in both the case when the switch is ON, and the case when the switch is OFF. Given the T/H's expected behavior, it is practical to summarizes the errors caused by the MOS non idealities into three main categories: 1) track mode errors, 2) hold mode errors, and 3) errors occurring during the track and hold modes transition (a.k.a. pedestal errors).

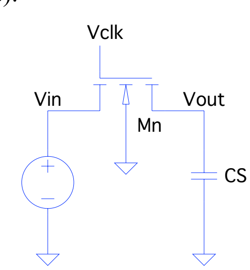

Fig. 1. Basic T/H circuit

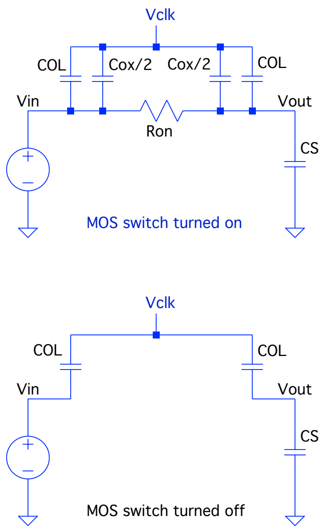

Fig. 2. Equivalent lumped models for T/H circuit

A. Track mode errors

There are three sources of error in track mode: 1) finite acquisition time, 2) thermal noise and 3) voltage dependence of the MOS switch.

Finite acquision time (i.e. finite bandwidth) is due to the switch non-zero resistance between drain and source ($\tau = R_{ON}C_S$), and results in both a transient residual error, and a steady state residual error. The transient error decay exponentially and can be reduced to any desired value by extending the length of the tracking phase. In a B-bit system, to achieve a transient residual error within 0.5×LSB, the tracking time $T_S/2$ has to be set to a value greater or equal to $\tau \times \ln(2^{B+1})$. The steady state residual error consists of a magnitude attenuation and a phase shift. This error depends on both the time constant of the T/H ($\tau = R_{ON}C_S$) and the frequency f_{in} of the input signal and it cannot be reduced by extending the length of the tracking phase. The percent amplitude error for a B-bit system with transient residual error within 0.5×LSB is equal to:

$$A_{err} = 1 - \frac{1}{\sqrt{1 + \left(\frac{\pi}{N}\frac{f_{in}}{f_S}\right)^2}} \tag{1}$$

where N is the ratio between the tracking time $T_S/2$ and the time constrant τ of the T/H circuit. For B=5, using N=4 while sampling at Nyquist rate ($f_{in}=f_S/2$) translates in about a 7% attenuation error. Although the estimated attenuation error may seem small, it is worth to notice that a 7% voltage drop across the non linear MOSFET's resistor does result in an unacceptable level of harmonic distortion. Precise tracking impose more stringent requirements (typically about 1% attenuation error). For achieving about 1% attenuation error at Nyquist rate (fin=fs/2) the ratio between tracking time and time constant must be set at about N=10.

Thermal noise is one of the most fundamental limitations that need to be addressed in the design of high speed T/H circuits [7]. By setting thermal noise and quantization noise to the same level it is possible to derive the following lower bound on the value of the sampling capacitance:

$$C_S \geq 12KT\left(\frac{2^B}{V_{FS}}\right)^2 \tag{2}$$

where V_{FS} is the full scale voltage of the ADC. Large values of C_S help reducing thermal noise, but requires the use of wide MOS switches in order to keep R_{ON} low enough to limit the sources of error that depends on the T/H time constant τ. Unfortunately wide MOS have large capacitances associated with them (i.e., large C_{OX} and C_{OL}), and as we will see this has a negative impact on two other sources of error: charge injection and clock feedthrough.

The MOS switch voltage dependence causes two problems: 1) the instant when the switch turn off (that is the sampling instant) is signal dependent and 2) the value of R_{ON} is non linearly dependent on the input signal V_{in}. The first problem can be effectlively minimized by making sure that the fall time T_f of the sampling clock is much faster than the maximum rate of change (dV_{in}/dt) of the input signal. Unfortunately the second problem is much harder to minimize and if not properly handled causes unacceptable levels of harmonic distortion. The non-linear dependency of R_{ON} on V_{in} is given by the following expression:

$$R_{ON} \approx \frac{1}{KP\frac{W}{L}\left(V_{gs} - V_{th}\right)} \approx \frac{1}{KP\frac{W}{L}\left(V_{clk} - V_{in} - V_{th}\right)} \tag{3}$$

The distortion caused by the non-linear dependency of R_{ON} on V_{in} is given by [8]:

$$HD_3 = \frac{Amplitude\ of\ third\ harmonic}{Amplitude\ of\ fundamental} \approx \approx \frac{1}{4}\left(\frac{A}{V_{GS} - V_{th}}\right)^2 \frac{f_{in}}{f_s}\frac{\pi}{N} \tag{4}$$

Where HD_3 is the third harmonic distortion, A is the amplitude of the input signal, and V_{GS} is the "quiescient" value of the gate-source voltage (i.e. the zero crossing of the sine input). From equation (4) is clear that for lowering distorsion the only two direct options are: 1) making the amplitude of the signal smaller than the overdrive voltage ($V_{OV}=V_{GS}-V_{th}$) and 2) making $1/\tau$ ($=2Nf_S$) much larger than $2\pi f_{in}$. Unfortunately both these options are impractical. Lowering the signal swing reduces the SNR of the system. Reducing τ requires the use of wide MOS switches and as already mentioned this implies large channel capacitance Cox and large overlap capacitance C_{OL}. The best strategy to reduce distorsion is to use an indirect technique known as gate-boosting. The basic idea behind gate boosting is to modulate the signal applied to the gate of the sampling switch ($V_g=V_{clk}$) with the input signal (V_{in}) so that V_{gs} becomes independent of V_{in}. If $V_g=V_{clk}+V_{in}$ then $V_{gs}=V_{clk}+V_{in}-V_{in}=V_{clk}$ and the dependency of R_{ON} on V_{in} cancel out (at least to first order).

B. Hold mode errors

There are three sources of errors in hold mode: 1) hold mode feedthrough, 2) aperture uncertainty and 3) hold mode drooping.

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Hold mode feedthrough is due to the parasitic capacitances of the MOS switch (that is the overlap capacitances between gate and drain and gate and source and the parasitic capacitance between drain and source). When the MOS switch is off due to these parasitic capacitances a small fraction of the input signal still reaches the output node (see fig. 3). Fortunately, as long as the driver of the clock signal has small enough output resistance the problem does not introduce a significant error. Furthermore, if necessary the error can be almost completely cancelled by using a T-switch structure. Fig. 4 illustrate a T-switch structure.

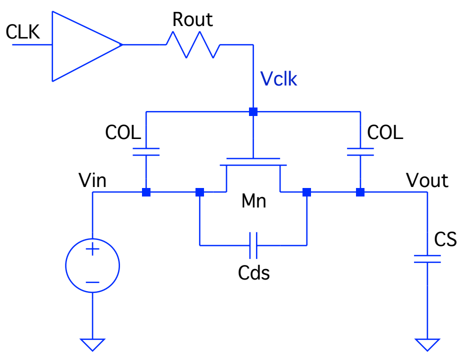

Fig. 3. Hold mode feedthrough mechanism

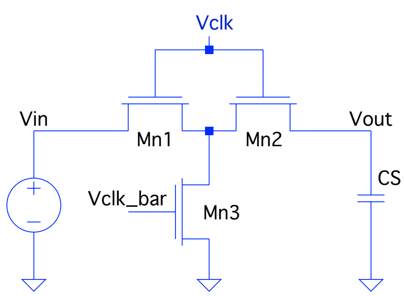

Fig. 4. T-switch structure

Aperture uncertainty is due to random timing variations in the actual sampling clock edge caused by the electronic noise. The error induced by the clock edge timing jitter is one of the fundamental issues limiting the performances of T/H circuits. The signal to jitter noise ratio achievable by a T/H circuit is given by [9]:

$$SNR_{aperture} = 20 \times log_{10}\left(\frac{1}{2\pi f_{in}\sigma_t}\right) \tag{5}$$

Where σ_t is the variance in the clock edge jitter (that is sqrt[E{Δt^2}]).

Hold mode drooping is due to the gate current leakage caused by the tunneling effect occurring when using technologies with ultra thin gate oxides [10]. The problem is releveant only for technologies smaller than 130nm and it is usually solved by using high-K dielectrics.

C. Pedestal errors

There are two mechanisms causing pedestal errors: 1) charge injection and 2) clock feedthrough.

Charge injection is due to the fact that when the sampling switch is suddenly turned off, part of the charge stored in the channel of the MOS is injected into the sampling capacitor C_S. This causes an offset in the voltage across the sampling capacitor. Assuming the charge is equally split between both sides of the MOS switch the offset is given by the following expression [11]:

$$\Delta V_{out} \approx -\frac{C_{OX}WL}{2C_S}(V_{DD} - V_{in} - V_{th}) \tag{6}$$

The exact amount of charge injected into the source side and the capacitor side depends on the impedances looking into both sides [12]. Due to its input dependent nature, charge injection is difficult to account for. A very effective strategy to reduce its effect is to use bottom sampling techniques.

Clock feedthrough is due to the fact that when the clock signal applied to the gate of the sampling switch goes off, the voltage variation at the gate of the MOS switch gets divided between the parasitic overlap capacitance C_{OL} and the sampling capacitor C_S causing an offset voltage across the sampling capacitor. Provided that the fall time of the clock is fast enough compared to the input signal the offset error is upper bounded by the following value:

$$\Delta V_{out} \approx -\frac{C_{OL}}{C_{OX} + C_{OL}}V_{DD} \tag{7}$$

Because charge injection and clock feed-through errors occur simultaneously it is difficult to analyze them separately [13]. Fortunately, in most cases clock-feedthrough is negligible compared to charge injection. However, even when this is not the case, as long as the clock's fall time is small, clock feed-through is input independent, so it can be easily cancelled out.

III. TRACK AND HOLD ARCHITECTURE

Fig. 5 shows the schematic of the T/H architecture used in our design. The architecture relies on bootstrapping [14] for limiting the distortion caused by the non-linearity of the MOS on-resistance and bottom plate sampling to limit the effect of charge injection [15]. To "eliminate" the non-linear fluctuation of the tracking switch's resistance with V_{in}, the voltage at the gate of M_{11} is boosted to V_{in}+V_{DD} so that ideally $V_{GS}(M_{11})$ would stay at a constatnt value V_{DD}. In practice, the efficacy of the bootstrap circuit is limited by trhe backgate effect of the tracking switch (transistor M_{11}) and the parasictic capacitance C_{par} at the top plate of the bootstrap capacitance C_{boot}. As a result the conductance of the tracking switch is:

$$G_{ON} = KP \cdot C_{OX} \cdot \frac{W}{L}\left(\frac{C_{boot}}{C_{boot} + C_{par}}V_{DD} - \frac{C_{par}}{C_{boot} + C_{par}}V_{in} - V_{th}[V_{in}]\right) \tag{8}$$

where $V_{th}[V_{in}]$ denotes that the threshold voltage of the tracking switch is dependent on V_{in}. For the circuit to work correctly, C_{boot} must be sufficiently large to supply charge to the gate of M_{11} and all parasitic capacitances in the charging path. In our design, the bootstrap capacitance is 2pF, which is approximately 5 times C_{par}.

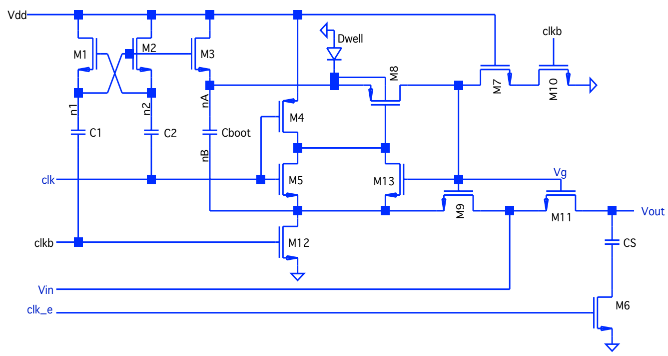

Fig. 5. T/H Architecture

The sizing requirements of the transistors and capacitors of the bootstrap circuit are quite relaxed. The sizes should be as small as possible for area consideration, but large enough to charge the various nodes at the desired voltage levels. The function of M_1, M_2, M_3, M_{12}, C_1 and C_2 is to charge C_{boot} to V_{DD} during the off phase (that is in hold mode). M_8 and M_9 affect the rise time of the voltage at the gate of the switch and M_7 and M_{10} affect the fall time. Bottom plate sampling is performed by turning off the switch M_6 earlier than the switch M_{11}. The capacitors have been implemented using MIM (Metal-Insulator-Metal). The track and hold time constant has been sized to achieve a 4% attenuation error at the Nyquist rate $f_{in}=f_s/2$. The input capacitance of each single comparator inside the 5-bit ADC is about 25fF, therefore the loading on the track and hold circuit due to the 31 required comparators is about 775 fF. Unfortunately, the input capacitance of the comparators varies non-linearly with V_{in}. To reduce the impact of this non-linearity we decided to add a fixed MIM capacitance C_S of 1pF at the output of the T/H circuit. Although a large value of C_S is beneficial for mitigating the non-linearity of the comparator's input capacitance, it increases the acquisition time (τ) of the T/H.

IV. SIMULATION RESULTS

The proposed architecture has been validated through SPICE simulation. The simulation results match well (within 10%) the analytical results obtained through MATLAB scripts. To optimize bandwidth all transistors have minimum channel length L=180nm. Table I summarizes the value of all devices employed in the design of the T/H. The diode (D_{well}) models the parasitic diode between n-well and p-substrate caused by the source-to-bulk connection of the PMOS transistor M_8. Fig.6 shows that the T/H is able to track and hold a differential input signal of frequency $f_{in}=f_s/2$ and amplitude V_{in}=1.3V. It takes about two clock cycles for the charge pump (that is M_1, M_2, C_1 and C_2) in the T/H circuit to start up bootstrapping the capacitance C_{boot} to V_{DD}.

V. CONCLUSIONS

This paper presents the design of a passive track and hold circuit based on bootstrapping and bottom plate sampling. The design is part of a 5-bit 8-fold time-interleaved ADC array. The sampling frequency achieved by each sub-ADC in the array is fs=300Msamples/s. The design has been implemented in a standard 180nm digital CMOS technology and it operates from a 1.8V supply. The circuit is able to track a differential input signal at Nyquist rate ($f_{in}=f_s/2$) and amplitude V_{in}=1.3V.

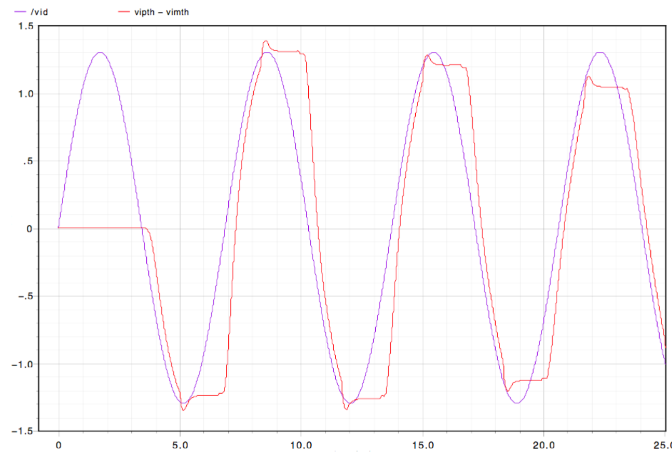

Fig. 6. Transient behavior of T/H circuit with $f_{in}=f_s/2$

TABLE I. T/H DEVICE SIZES

Device	Sizing
C1=C2 [fF]	200
C_{boot} [fF]	2000
C_S [fF]	1775
M1=M2 [µm]	L=0.18, W=5
M3=M12 [µm]	L=0.18, W=10
M4=M5 [µm]	L=0.18, W=5
M7=M10=M13 [µm]	L=0.18, W=0.36
M8 [µm]	L=0.18, W=1
M9 [µm]	L=0.18, W=5
M11=M6 [µm]	L=0.18, W=12.5
Dwell [µm]	Lwell=0.18+2, Wwell=1+2

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Electronic Speed Variator for a Brushless DC Motor

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***Abstract*—**In this paper the development of an electronic speed variator for a Brushless DC (BLDC) motor is presented. The speed variator is comprised of several blocks which include a power amplifier, an angular position sensing based on Hall Effect sensors, a voltage regulator and digital processing and data generation. The main characteristic of this work is that it is not based on the use of predesigned commercial components giving the basis for the development of new ideas. Also, it is possible to extend this work for broader range of BLCD motors and applications such as medicine, remote operating vehicles (ROVs) and general industrial uses.

***Keywords*—**Speed variator, brushless DC motor.

I. Introduction

THE idea behind the design of the speed variator is to design, construct and control a ROV quadcopter which obviously requires to regulate the speed of the propellers brushless DC motors. The trajectory control of unmanned aerial vehicles (UAV) has received great attention in the past years. In particular, the trajectory control of quadcopters, [].

In order to achieve this objective, it is necessary to design and construct appropriate actuators to manipulate the propellers speed and consequently the forces and torques that control the trajectory or flight path of the quadcopter. The speed variator must have appropriate time responses such that it can be inserted –as an actuator- in a control loop. From the academic perspective a second objective of this project is to generate the required knowledge to extend the design of speed variators for higher power BLDC motors.

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II. General Description

The system capable to regulate the speed of each of the 4 motors of a quadcopter is based on three blocks with different tasks: the first, dedicated to data processing; the second to signal conditioning, and the third a power driver. That is, the system is a three-phase driver powered by a DC voltage source which generate three PWM voltage signals required to operate a three poles BLDC motor, as shown in Figure 1, [1, 2]. It should be noted that the rotors speed is proportional to the commutation frequency of the three-phase inverter.

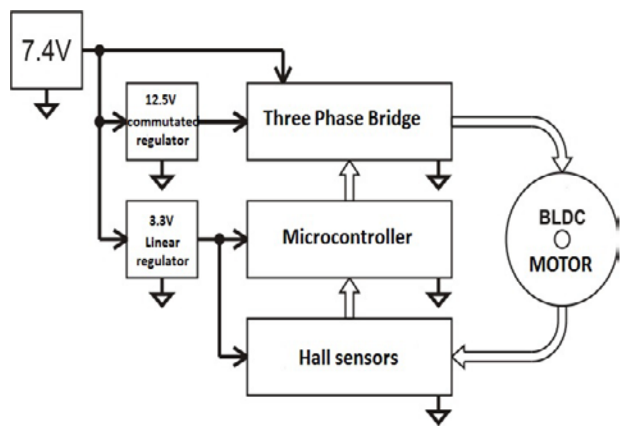

Fig. 1 Simplified Block Diagram

The 7.4 voltage source is a rechargeable LiPo battery with 2 cells is series. The microcontroller and the Hall Effect sensors are powered by a linear regulator L4931ABD33 from National Instrument. This regulator has an output of 3.3 volts and is powered by the 7.4 volts source. The three-phase inverter requires a source of 12 volts to feed the signal conditioning circuits and the power transistors. The 12 volts source is based on the commuted regulator LT1372 from Linear Technology. It was configured to generate 12.5 volts and is also powered by the LiPo battery.

To sense the rotors position 3 Hall Effect sensors US1881KUA from Melexis are allocated around the rotor to detect the magnetic field of its permanents magnets, Figure 2. These are “open-drain” sensors; therefore, its 3.3 volts polarization is by means of pull-up resistances. Each of the three signals is then led to the microcontroller

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dsPIC33FJ12MC202 [3, 4] from Microchip which is constantly monitoring these signals.

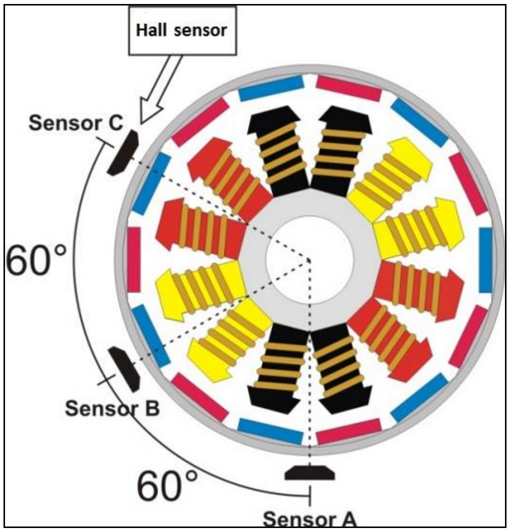

Fig. 2 Hall sensors positioning

Also, the microcontroller generates [3, 4], at the same time, the 6 signals that through the three-phase inverter control the high power transistors. In the three-phase inverter these signal are conditioned to comply with the level of current and voltage required by the high power transistors. The three-phase inverter generate in its output nodes Phase A, Phase B and Phase C (Figure 3) which are the signals for the *Energized Phase Sequence* (EPS), Figure 4.

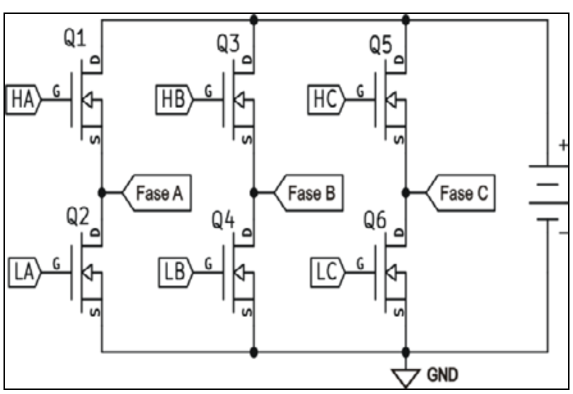

Fig. 3 Three-Phase inverter scheme.

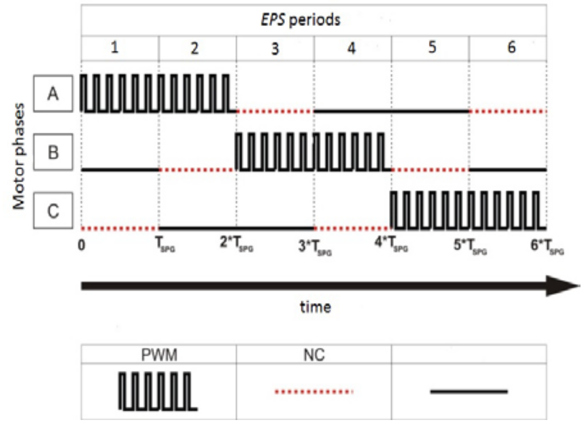

Fig. 4 EPS periods

The DC motor is the ZS2209-30 BLDC [5] out-runner three-phase from Hyperion, shown in Figure 5. When the motor is powered by the inverter its rotor spins producing changes in the Hall Effect sensors signals which subsequently close the feedback loop associated to the operation of the speed variator system.

Fig. 5 ZS2209-30 BLCD Motor

III. General Development

A. BLDC Motor operation

The Brushless DC motors (BLDC) are permanent magnets synchronous motors (PMSM). The magnets, normally refer as poles, are allocated in the rotor meanwhile the windings are in the stator, Figures 6 and 7. This kind of motors does not have commutators or mechanical switchers; therefore, they require an inverter or an electronic commuter to switch the DC power [1, 2] to the stator windings.

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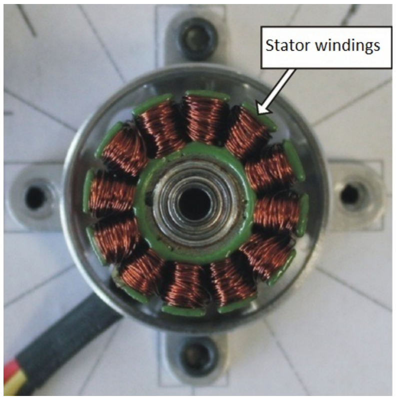

Figura 6. Motors stator windings

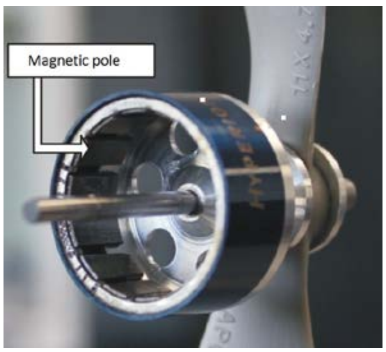

Figura 7. Motors magnetic poles

As mentioned above, to activate a BLCD motor is necessary to power, electronically with a specific sequence [5], the 3 phases of the motor with a DC voltage. The specific sequence is in fact the action effectuated by the mechanical switch in the case of motors with brushes. Because the BLCD motor is also a PMSM the rotors speed is proportional to the frequency of commutation. Moreover, the magnetic force by which the stator windings attracts the rotors poles is proportional to the average of the input voltage; hence, during the period of time in which each of the phases is activated they are not connected directly to the DC source

B. *Rotor's position sensing*

To detect the actual angular position of the rotor 3 sensors with Hall Effect are allocated around the rotor with a separation of 60° (Figure 2). Each sensor must be positioned between 2 stator windings of any of the 3 windings sets (Figure 2).

Each spin step of the *Rotor Spin Partial Sequence* (RSPS) generates changes in the output signals of some of the Hall Effect sensors. Therefore, for each step there is a unique combination of these 3 signals as shown in Table 1.

RSPS	Sensor A	Sensor B	Sensor C	
1	Sur	Sur	Sur	SSS
2	Norte	Sur	Sur	NSS
3	Norte	Norte	Sur	NNS
4	Norte	Norte	Norte	NNN
5	Sur	Norte	Norte	SNN
6	Sur	Sur	Norte	SSN

Table 1 Sensors signals for the 6 RSPS steps

Each of the two possible polarities detected by the Hall Effect sensors corresponds to a discrete voltage signal at its outputs. Figure 8 shows a graphic representing these signals.

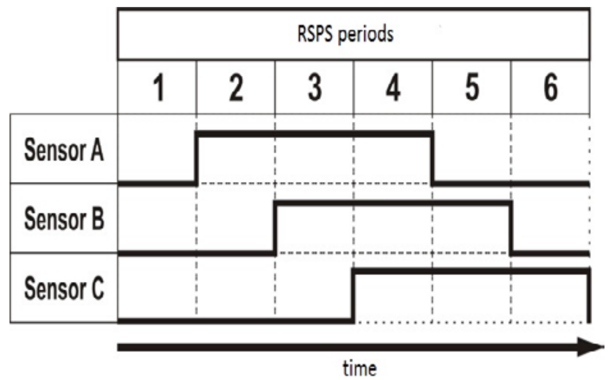

Fig. 8 RSPS periods graphic

Detecting the rotors angular position is necessary to determine the exact instant in which the EPS must be incremented in order to maintain the rotor spinning continuously.

C. *EPS Electric Signals*

To revolve the rotor at a constant angular velocity it is necessary to constantly repeat the EPS and each of its 6 steps (Table 1) must last enough time in order to induce a rotors angular displacement from an actual position to the next position. Hence, the RSPS period is equal to $\boldsymbol{6T_{RSP}}$, where T_{RSP} is the time of one step of the ESPS. This time is equal to total time duration of the EPS. Therefore, the total time of one spin of the rotor is then:

$$T_R = (T_{RSP})(6)(7)\ sec \tag{1}$$

Therefore, the average angular velocity is:

$$\omega = \frac{1}{T_R} = \frac{1}{(T_{RS})(6)(7)} \quad rad / sec \tag{2}$$

That is, to complete a rotation of 360° it is necessary to fulfil 7 RSPS. It must be noted that the real T_{RSP} is calculated based on the Hall Effect sensor information.

The PWM duty cycle (DuC) depends on the average voltage required in the phase during the fraction of time it is active. The average voltage is defined according to a desired constant velocity. This applies only for steady state conditions.

The RSPS signals are generated by the three phase inverter. This receives logic input signals from a microcontroller and generates similar output signals but upgraded in voltage and current. These signals are referred as Power-Signals.

IV. Experimental Results

The speed variator electronic circuits and the experimental set up are shown in Figures 9, 10 and 11, respectively.

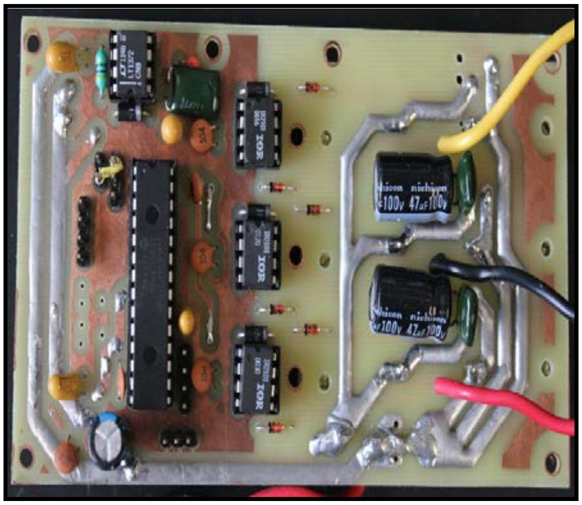

Fig. 9 Upper side of the speed variator circuit

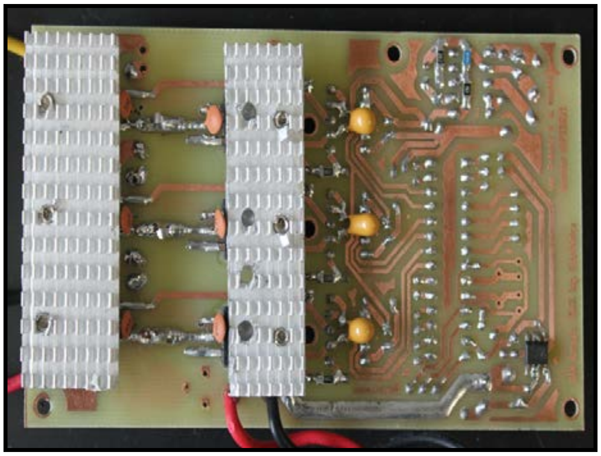

Fig. 10 Lower side of the speed variator circuit

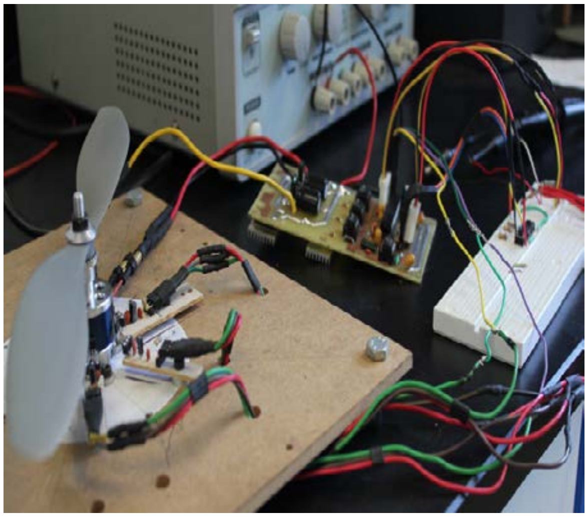

Fig. 11 Experiment Set Up

To show the experimental results and the effectiveness of the speed variator, the Power-Signal where displayed by pairs in a two channel oscilloscope. The 9 pairs of signals analyzed were:

1. LA and HA
2. LA and HB
3. LA and HC
4. LB and HA
5. LB and HB
6. LB and HC
7. LC and HA
8. LC and HB
9. LC and HC

After the interconnection of the sensors, motor, main board and oscilloscope, the system was turned on and the microcontroller run its program as expected:

a. During a period of one sec. the motor stand still. This is the programmed safety delay.
b. After the safety delay, the rotor is aligned to the stator to the position 1 of the RSPS (Figure 8)
c. Once the rotor is aligned to the stator it slowly starts to spin up to a constant velocity

In Figure 12, the pair of signals LA and Ha capture in the oscilloscope is shown.

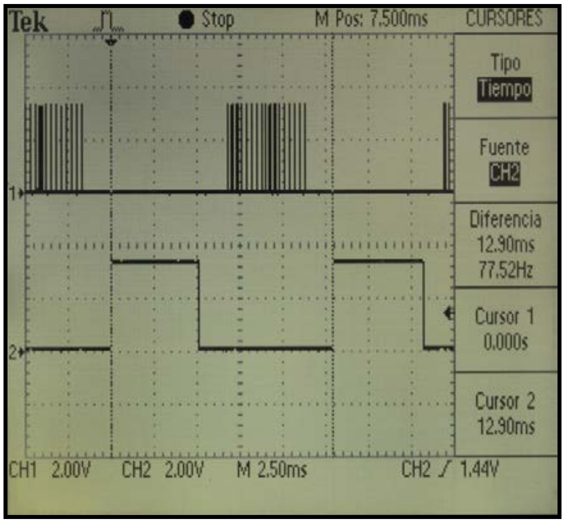

Fig. 12 LA and HA signals

In figure 13, signals LA and HA are display overlapping a visual guide to clearly distinguish each of the 6 step of the inverter sequence (IS)

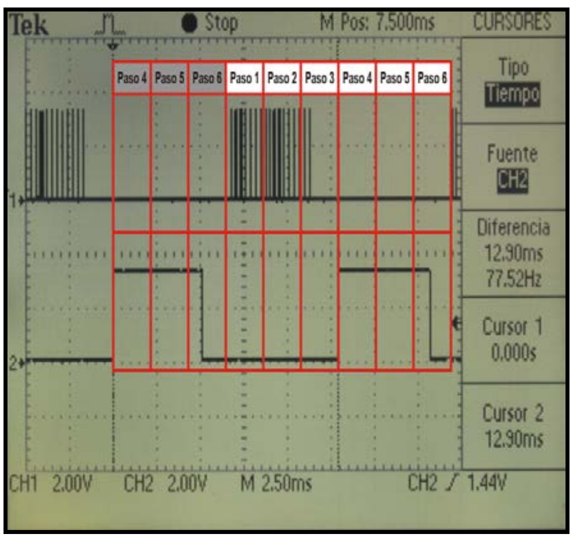

Fig. 13 LA and HA signals together with the inverter sequence

The microcontroller program responds to 3 user's commands:

a. Speed increment.
b. Speed decrement.
c. Stop

These buttons are allocated in the protoboard shown in Figure11

V. CONCLUSION

In this paper the design, construction and experimental tests of an electronic speed driver are presented. One of the most important aspects of design is that it is not based on the use of predesigned commercial components. It was found that a precise location of the Hall Effect sensors around the rotor is crucial to achieving high speeds. Due to its compact design it was possible to implement four of these drivers in a quadcopter without a significant payload increment.

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Improved Design of Optimal Narrow Band-Pass FIR Filters

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***Abstract*—This paper presents an improved design of optimal narrow band-pass FIR filters. In contrast to previous works, the narrow band-pass FIR filters are additionally specified by the pass-band properties which are reflected by a novel degree equation. The degree equation relates the filter specification and the filter length. The enhanced filter design procedure is presented. One example demonstrates its functionality and robustness.**

Keywords*—*degree equation, FIR filter, narrow filter, band-pass filter, equiripple approximation.

I. Introduction

Narrow band-pass filters are an useful tool for separation of a narrow band of frequencies in various applications. If an unconditional stability and linear phase are required, the digital finite impulse response (FIR) filters are the only choice. An unique class of FIR filters is represented by equiripple (ER) FIR filters. They exhibit the lowest possible filter length for arbitrary filter specification. In [1] the closed form design of narrow ER band-pass FIR filters was presented. It is based on an approximating function which is common to both ER notch [2] and band-pass FIR filters. In [1] the narrow ER band-pass FIR filter is specified by the central pass-band frequency and by the attenuation in stop-band related to the width of the stop-band. Here we present an improved design which additionally includes the attenuation in the pass-band related to the width of the pass-band. Finally, we present a novel degree equation which also includes the band-pass filter specification. An essential advantage of the presented closed form design is its superiority over the numerical Parks-McClellan/Remez design. It is functional even when the numerical approach does not converge.

II. Zero Phase Transfer Function

We assume an impulse response $h(k)$ with odd length $N = 2n+1$ coefficients and with even symmetry

$$a(0) = h(n)\ ,\ a(k) = 2h(n-k) = 2h(n+k)\ ,\ k = 1 \ldots n\,. \tag{1}$$

The transfer function $H(z)$ of the filter is

$$H(z) = \sum_{k=0}^{2n} h(k)\, z^{-k} = z^{-n} \sum_{k=0}^{n} a(k)\, T_k(w) = z^{-n} Q(w) \tag{2}$$

where $T_m(w)$

$$T_k(w) = \cos(k \arccos(w)) \tag{3}$$

is Chebyshev polynomial of first kind and the function

$$Q(w) = \sum_{k=0}^{n} a(k)\, T_k(w) \tag{4}$$

represents a polynomial in the variable $w = (z+z^{-1})/2$ which reduces on the unit circle $z = e^{j\omega T}$ to the real valued zero phase transfer function (ZPTF) $Q(w)$ of the real argument $w = \cos(\omega T)$.

III. Generating Function

Each particular approximation of the frequency response of a filter is based on a particular generating function. The generating function of a narrow ER BP FIR filter is the equiripple polynomial $Z_{p,q}(w,\kappa)$ which is advantageously expressed in terms of Jacobi elliptic Eta function $H(x,\kappa)$, see e.g. eq. (27) in [2] or its more elaborated form (5) here. The generating polynomial $Z_{p,q}(w,\kappa)$ approximates a constant value corresponding to the stop-band of an ER BP FIR filter in equiripple Chebyshev sense in two separated intervals $(-1, w_{s1})$ and $(w_{s2}, 1)$, see Fig. 1. The quantity $\mathbf{K}(\kappa)$ is the quarter-period and $F(x,\kappa)$ is the incomplete elliptic integral of the first kind, see also [2]. The main lobe of the generating polynomial is located inside the interval (w_{s1}, w_{s2}) and its maximal value is $y_m = Z_{p,q}(w_m,\kappa)$. The notation $Z_{p,q}(w,\kappa)$ emphasizes the fact that the integer value p counts the number of zeros right from the maximum w_m and the integer value q corresponds to the number of zeros left from the maximum w_m (Fig. 1). The real valued Jacobi elliptical modulus $0 < \kappa < 1$ affects the maximum value y_m and the width of the main lobe. For increasing κ the value y_m increases and simultaneously the main lobe broadens. The degree of the generating polynomial (5) is $n = p+q$. The position w_m of the maximum value $y_m = Z_{p,q}(w_m,\kappa)$ of the main lobe is

$$\begin{aligned} w_m = 1 + 2\,\mathrm{sn}\left(\frac{p}{n}\mathbf{K}(\kappa),\kappa\right) \mathrm{cd}\left(\frac{p}{n}\mathbf{K}(\kappa),\kappa\right) \mathrm{Z}\left(\frac{p}{n}\mathbf{K}(\kappa),\kappa\right) \\ -2\,\mathrm{sn}^2\left(\frac{p}{n}\mathbf{K}(\kappa),\kappa\right)\ , \end{aligned} \tag{6}$$

the edges of the main lobe are

$$w_{s1} = 1 - 2\,\mathrm{sn}^2\left(\frac{p}{n}\mathbf{K}(\kappa),\kappa\right) \tag{7}$$

$$w_{s2} = 2\,\mathrm{sn}^2\left(\frac{q}{n}\mathbf{K}(\kappa),\kappa\right) - 1 \tag{8}$$

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$$Z_{p,q}(w,\kappa)=\frac{(-1)^p}{2}\left[\left(\frac{H\left(F\left(\mathrm{sn}\left(\frac{p}{n}\ \mathbf{K}(\kappa),\kappa\right)\sqrt{\frac{1+w}{w+2\,\mathrm{sn}^2\left(\frac{p}{n}\mathbf{K}(\kappa),\kappa\right)-1}},\kappa\right)-\frac{p}{n}\ \mathbf{K}(\kappa),\kappa\right)}{H\left(F\left(\mathrm{sn}\left(\frac{p}{n}\ \mathbf{K}(\kappa),\kappa\right)\sqrt{\frac{1+w}{w+2\,\mathrm{sn}^2\left(\frac{p}{n}\mathbf{K}(\kappa),\kappa\right)-1}},\kappa\right)+\frac{p}{n}\ \mathbf{K}(\kappa),\kappa\right)}\right)^n\right.$$
$$\left.+\left(\frac{H\left(F\left(\mathrm{sn}\left(\frac{p}{n}\ \mathbf{K}(\kappa),\kappa\right)\sqrt{\frac{1+w}{w+2\,\mathrm{sn}^2\left(\frac{p}{n}\mathbf{K}(\kappa),\kappa\right)-1}},\kappa\right)+\frac{p}{n}\ \mathbf{K}(\kappa),\kappa\right)}{H\left(F\left(\mathrm{sn}\left(\frac{p}{n}\ \mathbf{K}(\kappa),\kappa\right)\sqrt{\frac{1+w}{w+2\,\mathrm{sn}^2\left(\frac{p}{n}\mathbf{K}(\kappa),\kappa\right)-1}},\kappa\right)-\frac{p}{n}\ \mathbf{K}(\kappa),\kappa\right)}\right)^n\right] \quad (5)$$

and $\mathrm{sn}(x,\kappa)$, $\mathrm{cd}(x,\kappa)$ are Jacobi elliptic functions. The relation for the maximum value y_m

$$y_m=\cosh 2n\left(\sigma_m \mathrm{Z}(\frac{p}{n}\mathbf{K}(\kappa),\kappa)-\Pi(\sigma_m,\frac{p}{n}\mathbf{K}(\kappa),\kappa)\right) \quad (9)$$

is useful in the normalization of the generating polynomial where the auxiliary parameter σ_m is given by the formula

$$\sigma_m=F\left(\arcsin\left(\frac{1}{\kappa\ \mathrm{sn}\left(\frac{p}{n}\ \mathbf{K}(\kappa)|\kappa\right)}\sqrt{\frac{w_m-w_{s1}}{w_m+1}}\right),\kappa\right)\ . \quad (10)$$

The generating polynomial $Z_{p,q}(w,\kappa)$ can be advantageously expressed in terms of its expansion into Chebyshev polynomials of first kind

$$Z_{p,q}(w,\kappa)=\sum_{k=0}^{n}a(k)T_k(w)\ . \quad (11)$$

The algorithm for an algebraic evaluation of the coefficients $a(k)$ was introduced in [3]. Finally, the ZPTF $Q(w)$ of the filter is represented by the normalized generating polynomial

$$Q(w)=\frac{1+Z_{p,q}(w,\kappa)}{1+y_m}=\frac{1+Z_{p,q}(w,\kappa)}{1+Z_{p,q}(w_m,\kappa)}\ . \quad (12)$$

IV. Degree Equation

The best frequency selectivity of the filter is obtained for the minimal width of its transition bands. The selective properties of the filter can be specified in particular bands independently. However, the filter specification cannot be met precisely in all bands at the same time as the dynamic properties of the frequency response in particular bands are interrelated and they are determined by the approximating function. Consequently we have to investigate the influence of the filter specification upon the filter degree both in the pass-band and in the stop-band. We will denote the values attributed to the pass-band resp. stop-band by the indices p resp. s. The ER BP FIR filter is specified by the pass-band frequency $\omega_m T=\mathrm{acos}(w_m)$, width of the pass-band $\Delta\omega_p T=(\omega_{p2}-\omega_{p1})T=\mathrm{acos}(w_{p2})-\mathrm{acos}(w_{p1})$, attenuation in the pass-band $a_{pdB}=20\log(a_p)$, width of the stop-band $\Delta\omega_s T=(\omega_{s2}-\omega_{s1})T=\mathrm{acos}(w_{s2})-\mathrm{acos}(w_{s1})$ and attenuation in the stop-band $a_{sdB}=20\log(a_s)$, see Fig. 2. We will evaluate a filter degree n_p related to the pass-band and a filter degree n_s related to the stop-band. In order to satisfy the filter specification the filter degree is $n=\max\langle n_p,n_s\rangle$. The filter length is $N=2n+1$ coefficients. Let us start with the stop-band. The filter degree n_s corresponding to the stop-band follows from the generating polynomial (5) and it is closely related to the degree of an equiripple notch FIR filter [2], namely

$$n_s=\frac{\ln\left(y_m+\sqrt{y_m^2-1}\right)}{2\sigma_m \mathrm{Z}\left(\sigma_s,\kappa\right)-2\Pi\left(\sigma_m,\sigma_s,\kappa\right)} \quad (13)$$

where $Z(x,\kappa)$ stands for Jacobi Zeta function and $\Pi(x,y,\kappa)$ for elliptic integral of third kind [2]. The value σ_s is

$$\sigma_s=F\left(\frac{\omega_m+0.5\Delta\omega_s}{2}T,\kappa\right)\ . \quad (14)$$

The elliptic modulus κ can be expressed in the form

$$\kappa=\sqrt{\frac{2\left[\cos(\omega_m-0.5\Delta\omega_s)T-\cos(\omega_m+0.5\Delta\omega_s)T\right]}{\left[1+\cos(\omega_m-0.5\Delta\omega_s)T\right]\left[1-\cos(\omega_m+0.5\Delta\omega_s)T\right]}}. \quad (15)$$

On the other hand, it is apparent, that the approximating polynomial (5) is not suitable for further algebraic manipulations and consequently for the derivation of the degree n_p because the Jacobi Eta function $H(x,\kappa)$ is a transcendental function and an explicit formula for its inversion is not known. We propose an alternative way for the derivation of the degree n_p which is based on the fact, that the widest pass-band $\Delta\omega_p T$ occurs always for the symmetrical case where the pass-band frequency is $\omega_m T=\pi/2$ ($w_m=0$), i.e. for $p=q$, and further on the fact, that the width of the pass-band $\Delta\omega_p T$ varies only slightly with the varying position of the pass-band frequency $\omega_m T$. For illustration of this facts see, Fig. 3. For $p=q$, the generating polynomial $Z_{q,q}(w,\kappa)$ is symmetric around $w=w_m=0$ (Fig. 4) and it reduces to the Chebyshev polynomial of first kind of a quadratic argument, namely

$$Z_{q,q}(w,\kappa)=(-1)^q T_q\left(\frac{2w^2-1-k'^2}{1-k'^2}\right) \quad (16)$$

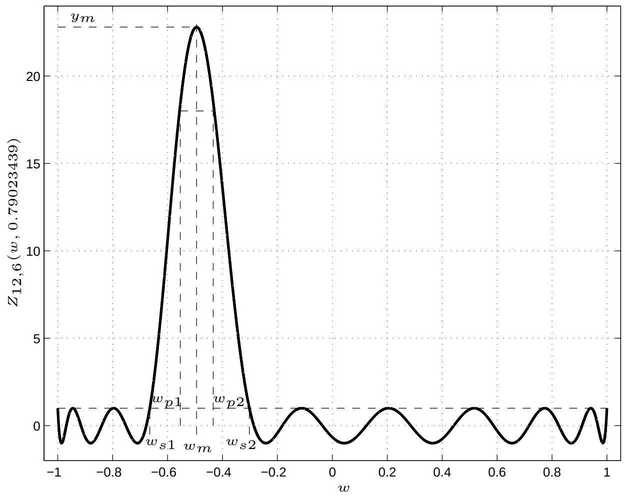

Fig. 1. Generating polynomial $Z_{12,6}(w, 0.79023439)$.

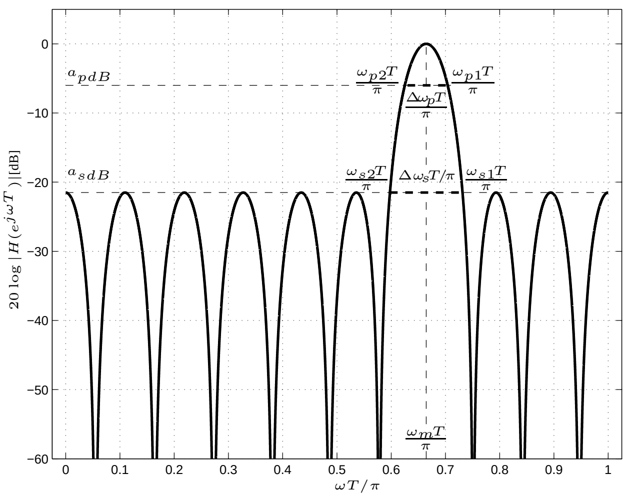

Fig. 2. Amplitude frequency response $20 \log |H(e^{j\omega T})|$ [dB] corresponding to the ZPTF $(1 + Z_{12,6}(w, 0.79023439))/(1 + Z_{12,6}(w_m, 0.79023439))$ based on the generating polynomial from Fig. 1.

where

$$k' = \frac{1-\sqrt{1-\kappa^2}}{1+\sqrt{1-\kappa^2}} = \frac{1-\kappa'}{1+\kappa'} \,. \tag{17}$$

For illustration, the normalized polynomial

$$\frac{Z_{q,q}(w,\kappa)+1}{y_m+1} = \frac{Z_{q,q}(w,\kappa)+1}{Z_{q,q}(0,\kappa)+1} = \frac{T_q\left(\dfrac{1+k'^2-2w^2}{1-k'^2}\right)+1}{T_q\left(\dfrac{1+k'^2}{1-k'^2}\right)+1} \tag{18}$$

for $q = 20$ and $k' = 0.1$ is shown in Fig. 4. The maximum value y_m of the polynomial $Z_{q,q}(w, \kappa)$ is located at $w = w_m = 0$ and its value is

$$\begin{aligned} y_m &= (-1)^q T_q\left(\frac{-1-k'^2}{1-k'^2}\right) = T_q\left(\frac{1+k'^2}{1-k'^2}\right) \qquad (19) \\ &= \frac{1}{2}\left[\left(\frac{1+k'}{1-k'}\right)^q + \left(\frac{1-k'}{1+k'}\right)^q\right] = \frac{1}{2}\left(\kappa'^q + \kappa'^{-q}\right). \end{aligned}$$

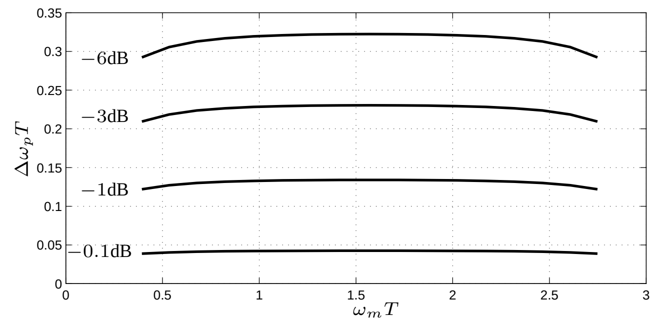

Fig. 3. Dependence of the width of the pass-band $\Delta\omega_p T$ on the pass-band frequency $\omega_m T$ of an equripple band-pass filter for $n = 20$ ($N = 41$), a_{sdB} =-60, a_{pdB}=-0.1, -1, -3 and -6.

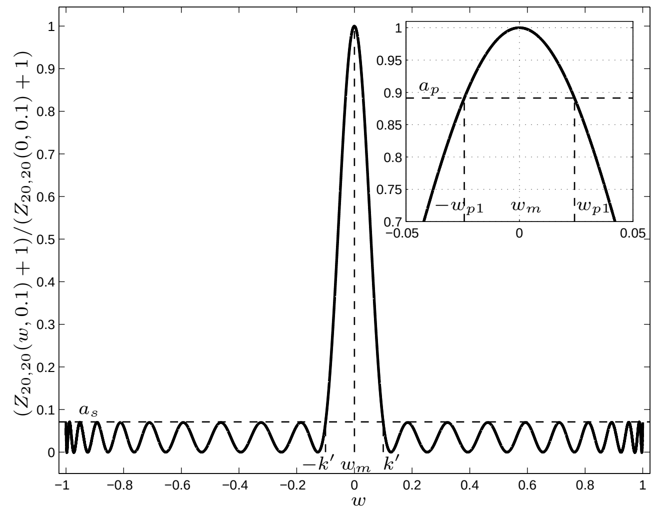

Fig. 4. Polynomial $\dfrac{Z_{20,20}(w,\, 0.1)+1}{Z_{20,20}(0,\, 0.1)+1}$ and a detailed view of its pass-band.

By inversion of (19) we get

$$k' = \frac{1-\left(y_m-\sqrt{y_m^2-1}\right)^{1/q}}{1+\left(y_m-\sqrt{y_m^2-1}\right)^{1/q}} \,. \tag{20}$$

It is apparent from the pass-band of the symmetric filter (Fig. 4) that

$$\frac{T_q\left(\dfrac{1+k'^2-2w_{p1}^2}{1-k'^2}\right)+1}{y_m+1} = a_p = 10^{a_{pdB}/20} \,. \tag{21}$$

Considering (21) and considering $w_{p1} = \cos[(\Delta\omega_p T + \pi)/2]$ we finally arrive at the degree equation of an ER BP FIR filter which reads

$$n_p = \frac{2\,\mathrm{acosh}\left(2.10^{(a_{p\,dB}-a_{s\,dB})/20}-1\right)}{\mathrm{acosh}\dfrac{1+k'^2-2\cos^2\frac{\Delta\omega_p T+\pi}{2}}{1-k'^2}} \,. \tag{22}$$

V. Design Procedure

The proposed algebraic filter design consists of a few steps as follows:

○ Specify the normalized (non-normalized) pass-band frequency $\omega_m T$ (f_m), width of the pass-band $\Delta\omega_p T$ (Δf_p), attenuation in the pass-bands a_{pdB}, width of the stop-band $\Delta\omega_s T$ (Δf_s) and the attenuation in the stop-bands a_{sdB} (Fig. 2). For the non-normalized frequencies specify additionally the sampling frequency f_s.

○ For the non-normalized frequencies evaluate their normalized values

$$\omega_m T = 2\pi \frac{f_m}{f_s} \ , \ \Delta\omega_p T = 2\pi \frac{\Delta f_p}{f_s} \ , \ \Delta\omega_s T = 2\pi \frac{\Delta f_s}{f_s} \ . \tag{23}$$

○ Calculate the stop-band edges

$$\omega_{s1} T = \omega_m T + \frac{\Delta\omega_s T}{2} \ , \ \omega_{s2} T = \omega_m T - \frac{\Delta\omega_s T}{2} \ . \tag{24}$$

○ Evaluate the Jacobi elliptic modulus κ (15).

○ Evaluate

$$\varphi_1 = \frac{\omega_{s1} T}{2} \ , \ \varphi_2 = \frac{\pi - \omega_{s2} T}{2} \tag{25}$$

and calculate the rational values

$$\frac{p}{n}\mathbf{K}(\kappa) = F(\varphi_1|\kappa) \ , \ \frac{q}{n}\mathbf{K}(\kappa) = F(\varphi_2|\kappa) \ . \tag{26}$$

○ Determine the required maximum value y_m of the main lobe $y_m = 2.10^{-0.05 a_s[dB]}$ (Fig. 1).

○ Calculate and round up the degree n_s (13) for the stop-band and the degree n_p (22) for the pass-band. The filter degree n is the maximum of both and the filter length is $N = 2n+1$ coefficients.

○ Calculate the integer values p and q of the generating polynomial $Z_{p,q}(w,\kappa)$

$$p = \left[n \frac{F(\varphi_1|\kappa)}{\mathbf{K}(\kappa)} \right] \ , \ q = \left[n \frac{F(\varphi_2|\kappa)}{\mathbf{K}(\kappa)} \right] \tag{27}$$

where the brackets [ ] in (27) stand for rounding.

○ For the values p, q, κ and y_m evaluate the impulse reponse $h(k)$ using Tab. V in [2] and eq. (1) here.

VI. Example of the Design

In order to demonstrate the robustness of the design, let us specify an extremely narrow ER BP FIR filter by the pass-band frequency $f_m = 10.7$ MHz, by the width of the pass-band $\Delta f_p = 1$ kHz for the attenuation $a_{pdB} - 3$ and by the width of the stop-band $\Delta f_s = 5$ kHz for the attenuation $a_{sdB} = -80$. The specified sampling frequency is $f_s = 30$ MHz.

Using formulas we get $\kappa = 0.05166139$ (15), $n_s = 20196$ (13), $n_p = 20248$ (22), i.e. $n = 20248$, further $p = 14444$ and $q = 5804$ (27). The filter length is $N = 40497$ coefficients. The actual filter selectivity is $\Delta f_{p\,act} = 1.21$ kHz for $a_{pdB} - 3$ and $\Delta f_{s\,act} = 4.99$ kHz for $a_{sdB} = -80$. The amplitude frequency response and the passband of the filter is shown in Fig. 5.

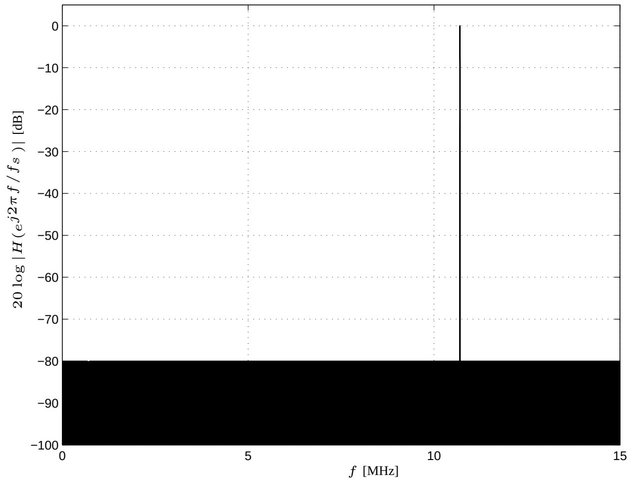

Fig. 5. Amplitude frequency response $20\log|H(e^{j2\pi f/f_s})|$ [dB].

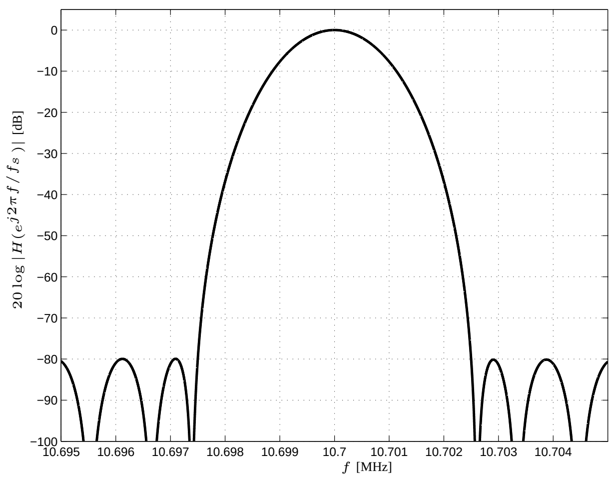

Fig. 6. Detailed view of the pass-band of the filter.

VII. Conclusions

We have presented an improved analytical design of narrow digital equiripple band-pass finite impulse response filters. In contrast to the established numerical design procedures the proposed design method is based on the approximating polynomial and provides a formula for the degree of the filter.

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Wireless Power Transfer through Inductive Coupling

Mohamed A. Hassan, A.Elzawawi

Abstract

Wireless power transfer is a new technology to transfer electrical power without any physical contact between the source and the load. The aim of this paper is to propose the use of a simple, cheap and easy technique for charging any mobile. The various technologies available so far for wireless transmission of electricity and the need for a wireless system of energy transmission are discussed here. The main problem is how power is transferred wirelessly without any bad effect on environment and human. The core of the used technology is making use of the magnetic resonance concept for transmitting the power wirelessly for charging any mobile. Electric power is transferred at a frequency of about 100 kHz in a short distance range to charge a mobile making use of resonance. An impedance compensating network is used to achieve maximum power transfer. The practical results are very close to these obtained using the mathematical model and the theoretical calculations. The new applications of wireless power transfer technology (WPTT) are enumerated in this paper.

Keywords wireless power transfer technology (WPTT), inductive power transfer (IPT), capacitive power transfer (CPT), magnetic resonance.

I. Introduction

The transfer of electric energy from a power source to an electric load without a direct physical connection between them, usually via an electromagnetic field, is defined as Wireless Power Transfer Technology (WPTT).

Nowadays, electronic devices such as cell phones and laptops need WPTT for wireless charging with also the advantage of the protection from any faults at the power source.

In the 1890's, a wireless power transfer (WPT) system was demonstrated by Nikola Tesla using his demonstration on resonant transformers called Tesla coils.

In July 2007, a group of researchers at MIT presented a method of transmitting power wirelessly [1].The researchers used an electromagnetically coupled resonance system to power a 60W light bulb wirelessly from a distance over two meters away. The magnetic resonance coupling technology has been found to be viable for midrange energy transfer. It is used for charging the electric vehicles with energy efficiency up to 90% in a relatively short time. It is also used for low power wireless charging of mobile phones with a power up to five watts and energy efficiency up to 70%.

II. Categories of wireless power transfer

Various methods used in WPTT mainly depend on the range between the transmitter and the receiver, operating frequency and the amount of transmitted power [2-5].

There are two fields of WPTT, Far Field WPTT (FFWPTT) and Near Field WPTT (NFWPTT). The main differences between the two types of fields are illustrated in Table I.

Table I
Main differences between FFWPTT and NFWPTT

WPT	Far Field	Near Field
Range	Long	Short-Mid
Phenomenon	Coupled mode theory	Induction theory
Frequency	Mega Hertz	Kilo Hertz
Efficiency	Low	High

FFWPTT is based on the electromagnetic radiation concepts which can be divided into microwave and laser according to the operating frequency. NFWPTT can be categorized as magnetic induction WPTT (MIWPTT) and electric induction WPTT (EIWPTT) .Energy transfer in MIWPTT depends on the mutual coupling between the coils which is known as inductive power transfer (IPT).In EIWPTT, energy is transferred through the electric field between the plates of the capacitor .This is known as capacitive power transfer (CPT). The main differences between the two induction methods are illustrated in Table II.

Table II
Comparison between IPT and CPT system

Technology	Performance		
	Efficiency	EMI	Frequency
Inductive Power Transfer (IPT)	Medium	Medium	10-50 kHz
Capacitive Power Transfer (CPT)	Low	Medium	100-500 kHz

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III. System Description

The WPT system consists of a power source which is a high speed switching circuit, primary impedance compensating network, two magnetically coupled coils, a secondary impedance compensating network, a high frequent rectifier, a voltage regulator and a DC load. The schematic diagram of WPT system is illustrated in Fig.1.

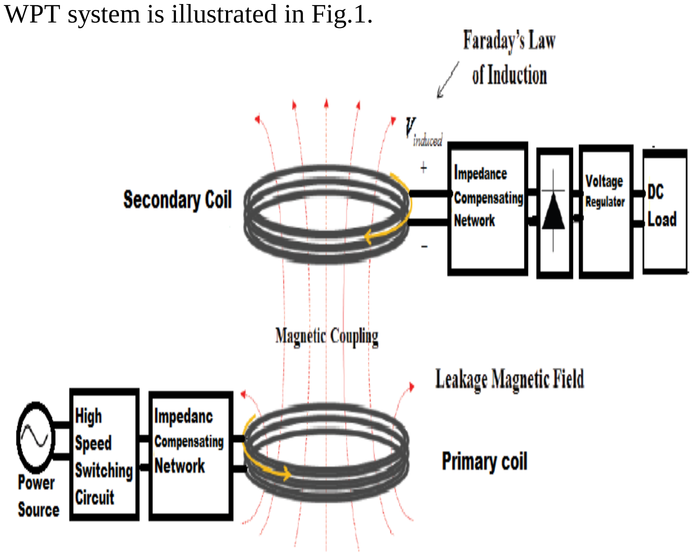

Fig. 1 Schematic diagram of WPT system

The high speed switching circuit is a single-ended high frequency quasi resonant inverter that consists of power MOSFETs and triggering circuits. A power MOSFET is a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) designed to handle significant power levels and can operate at high frequencies up to hundreds of kilo Hertz. Now, the power electronics development reaches to a new power MOSFET (SiC MOSFET) that can operate at frequencies up to Mega Hertz which is used for high switching frequency applications [6].

The impedance compensating network (matching network) has a very important role in WPT system .It reduces the volt-ampere rating of the power source by minimizing the reactance of input impedance and increase the power transfer efficiency by utilizing the magnetic field resonance.

The time varying magnetic field is generated from the primary coil and is gathered at the secondary coil to transfer the average load power [7-8].

A high frequency rectifier is used to convert high frequency AC power into a DC power. There are two lose contributions associated with the diodes in a high frequent rectifier; losses due to the forward conduction of the diodes and the high frequent loss according to the switching time of the diodes. These losses act as a consequence of the reverse recovery time of the diodes. To eliminate the loss effect, Schottky diodes or ultrafast diodes are used in the rectifier circuit instead of normal diodes [9].

The voltage regulator is used to stabilize and control the DC voltage level according to the required load voltage.

The load is generally an electrical load that consumes certain electric power. The mobile battery is a common load in a WPT system as charging a mobile wirelessly means no need to connect the mobile charger to a mobile phone. The mobile phone is put on the charging pad and the charging operation starts till the phone is fully charged. The transfer circuit is attached to the charging pad and the receiving circuit is included inside the mobile.

The Wireless charging for a mobile via inductive coupling is illustrated in Fig.2.

Fig. 2 Inductive coupling between charging pad and phone

IV. Mathematical Model

The mathematical model of the wireless power transfer system through inductive coupling method is illustrated in this section.Fig.3 shows the simplified equivalent circuit model of the wireless power transfer system with two series resonant coils. The load power is increased by increasing by the frequency or the mutual inductance or the magnitude of source current [10].

The loop equations of the equivalent circuit are given by:

$$V_1 = Z_1 I_1 - j\,\omega M I_2 \qquad (1)$$

$$|I_2| = \frac{\omega M}{Z_2} I_1 \qquad (2)$$

As, V_1 is the supply voltage. I_1 and I_2 are the passing currents in the primary and secondary coils, respectively. Z_1 and Z_2 are the equivalent impedances of the transfer and receiving circuits, respectively. M is the mutual coupling between the two coils and depends on the coupling coefficient between them and the self INDUCTANCES l_1 AND l_2.

$$M = k\sqrt{l_1 l_2} \qquad (3)$$

At resonance frequency the equivalent impedances Z_1 and Z_2 can be simplified and approximated to

$$Z_1 = R_s + R_{1ac} \qquad (4)$$

$$Z_2 = R_l + R_{2ac} \qquad (5)$$

Where R_{1ac} and R_{2ac} are the series resistances of the primary and secondary coils, respectively. R_s and R_l are the source and load resistances, respectively.

The resonant frequency ω is defined as

$$\omega = \frac{1}{\sqrt{l_1 c_1}} = \frac{1}{\sqrt{l_2 c_2}} \qquad (6)$$

The load power can be deduced as

$$P_l = \frac{\omega^2 M^2}{(R_l + R_{2ac})^2} I_1^2 R_l \tag{7}$$

The power transfer efficiency is given by

$$\eta = \frac{\omega^2 M^2 R_l}{(\omega^2 M^2)(R_l + R_{2ac}) + (R_s + R_{1ac})(R_l + R_{2ac})^2} \tag{8}$$

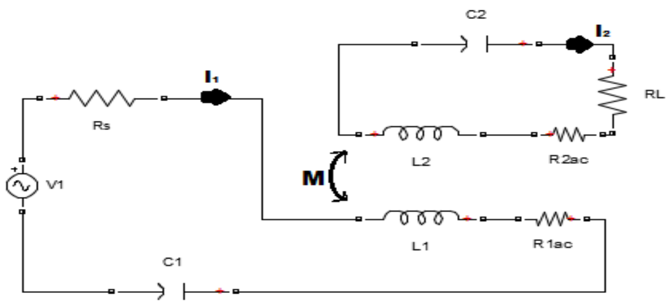

Fig. 3 Equivalent circuit of series-series resonance wireless power transfer system

From equations (7) and (8), the load power increases by increasing the frequency or the mutual inductance or the magnitude of source current. From equation (8), the efficiency increases by decreasing the parasitic resistance, increasing the frequency and the mutual inductance.

The losses due to the parasitic resistance R_{1ac} and R_{2ac} can be decreased by using Litz wire in coils design. Litz wire is used to mitigate the skin and the proximity effects. Generally, coupling is the interaction between two devices or circuits. The phenomenon of energy coupling explains how electrical energy is transferred from one device to another. When the interaction between the couplers is due to the magnetic field of one of the couplers, the coupling is known as a magnetic coupling. In magnetic coupling, the magnetic field of one of the devices induces current in the other device of the coupling system. Therefore, power can be transferred from a sending unit to a receiving one. The more flux reaches the receiver; the better the coils are coupled. The degree of coupling is expressed by the coupling factor k. From equation (3), it is clear that the coupling coefficient k depends on the medium between the two coupled coils and their parameters such as the number of turns, cross section area and coils lengths. In wireless charging the relative permeability is one. The use of two identical coils with a small spacing between them relative to the coils diameters ensures large coupling coefficient between them [11-12]. By increasing the coupling coefficient between the two coils, the power transfer efficiency will increase as illustrated in Fig.4.

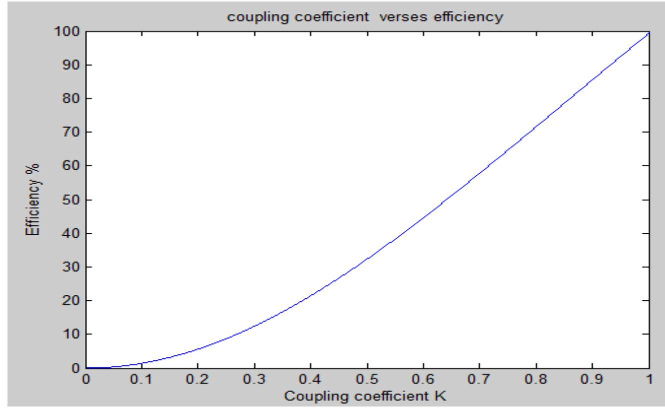

Fig.4 Relation between coupling coefficient and the power transfer efficiency in the simplified wireless charging model

V. EXPERIMENTAL WORK

The transfer coil is connected to the power source through a high speed switching circuit which operates at 112 kHz and a compensating network to achieve the resonance in the primary circuit. The receiver coil is connected to a mobile phone Nokia N70 through three stages. The first stage is a compensating network to maximize the induced current at the secondary by a series capacitor with the receiving coil. The second stage is a high frequent full wave rectifier designed using group of four Schottky diodes. The last stage is a voltage regulator and a charging system. The wireless charging system for a mobile Nokia N70 is illustrated in Fig.5.

Fig.5 Wireless charging system for Nokia N70

Fig.6 shows the relation between the load power and the loss power in the receiver circuit verses the angular frequency. It is clear that the maximum transferred power is achieved at the resonance frequency around w=700k rad/s related to the operating frequency of 112 kHz.

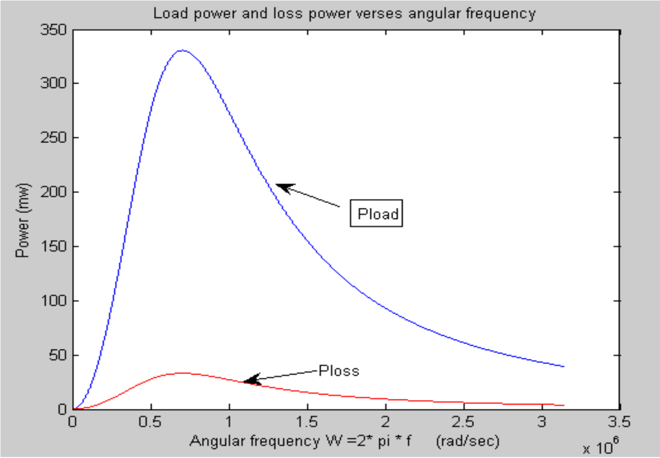

Fig.6 Load power and loss power distribution versus ω

VI. Applications of WPTT

There are many applications of WPTT such as:
1- Automatic wireless charging of mobile electronics
2- Robots, packaging machinery, assembly machinery and machine tools can take advantage of this technology.
3- Direct wireless power for wireless sensors and actuators, eliminates the need for expensive power wiring or battery replacement and disposal.
4- Automatic wireless charging for future hybrid and all-electric passenger and commercial vehicles, at home or in parking garages.
The IPT system is the world's first commercially wireless electric car charging system. It is described as the safest, most efficient and most effective way to transfer power without wires. The Wireless electric vehicles charging system is illustrated in Fig.7.

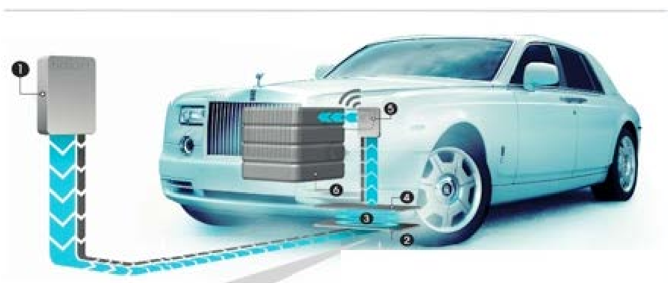
Fig.7 Wireless electric vehicles charging system

VII. Conclusion

Wireless mobile charging is an application of low power, short range WPTT .Our simplified model depends on series-series (SS) topology to transfer the needed power for charging inductively at resonance frequency with high coupling coefficient. The future work will be more development of this model to be of lower cost, efficient, simpler and compatible with any mobile.

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Acknowledgment

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Oscillator and Chaotic System Based on State Space Energy Feedback

M. Stork

Abstract **—**In this paper a new design method based on state energy concept is proposed. It is shown that linear system controlled by a linear controller with energy feedback can generate different types of signals. Depending on parameters of the controller the generated output signal can be sinusoidal, non-sinusoidal or even chaotic. The chaotic attractors are highly complex nonlinear dynamical systems. A new chaotic attractor was found by state space energy feedback. Spectral analysis shows that the system in the mode has very broad frequency bandwidth, and indicating the prospect for engineering applications e.g. secure communications, biology, etc.

Keywords **—** State energy; nonlinear; error feedback; dissipation; sinusoidal oscillator; chaotic system.

I. Introduction

CHAOS is a field in mathematics which has found wide application around us. Chaos theory studies the behavior of dynamical systems which are nonlinear, highly initial condition sensitive, having deterministic (rather than probabilistic) underlying rules which every future state of the system must follow. Such systems exhibit aperiodic oscillations in the time series of state variables. It has a large or infinite number of unstable periodic patterns which is commonly termed as order in disorder. Long term prediction is almost impossible due to the sensitive dependence on initial conditions. Though such effect may seem quite unusual but it is however observed in very simple systems, for example, a ball placed at the crest of a hill might roll into different valleys depending on slight difference in the initial position. Most common chaotic phenomenon is observed in case of regular weather prediction. Other application of chaos theory is pervaded in many fields like geology, mathematics, biology, microbiology, computer science, economics, philosophy, politics, population dynamics, psychology, robotics etc. Some real world applications of chaotic time series are computer networks, data encryption, information processing, pattern recognition, economic forecasting, market prediction etc. In this paper it will shown that linear system controlled by a linear controller with energy feedback can generate required types of signals. Depending on parameters of the controller the generated output signal can be sinusoidal, quasi-periodic or even chaotic.

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II. The State Space Energy Approach

Let's consider a class of *finite dimensional nonlinear systems* described in the following *form*

$$\begin{aligned} \dot{x} &= A(x)x + Bu \\ y &= C(x)x \end{aligned} \tag{1}$$

where the matrix *C(x),* defining the *output measurement*, is *not a"priori specified,* and the *structure* of matrices *A(x)* and *B* reads

$$A_n(x)=\begin{bmatrix} -\alpha_1 & \alpha_2 & 0 & 0 & 0 & 0 \\ -\alpha_2 & 0 & \alpha_3 & 0 & 0 & 0 \\ 0 & -\alpha_3 & 0 & \ddots & . & . \\ . & . & \ddots & \ddots & \alpha_{n-1} & 0 \\ 0 & 0 & 0 & -\alpha_{n-1} & 0 & \alpha_n \\ 0 & 0 & 0 & 0 & -\alpha_n & 0 \end{bmatrix};B_n=\begin{bmatrix} 1 \\ 0 \\ . \\ . \\ 0 \\ 0 \end{bmatrix} \tag{2}$$

We start with presentation of some *basic ideas* of the *state space energy based* approach [1, 2, 3, 4, 5]. Let $P_0(t)$ denotes the *output dissipation power* of a *zero input causal system* with an *informational output y(t)* defined by

:

$$y(t) = \pm\sqrt{P_0(t)},\, P_0(t) \geq 0 \tag{3}$$

Let *E(t)* denotes the *instantaneous value of the state space energy* (stored in a state vector *x(t)*):

$$E(t) = \int_{t_0}^{\infty} P_0(\tau)d\tau,\ \forall t:\ t = t_0 \tag{4}$$

The state space energy conservation principle holds

$$\frac{dE}{dt} = \langle \psi(x), f(x) \rangle = -P_0(t) \tag{5}$$

where ψ is the gradient vector of the state space energy potential field E, f is the state space velocity vector, and $\langle .,. \rangle$ denotes the operation of dual product.

Because the choice of origin and that of the state space coordinate system is free we can define the gradient $\psi(x)$ of the energy E in its most simple form:

$$\psi(x) = x^T \rightarrow E = \frac{1}{2}\sum_{i=1}^{n} x_i^2 \tag{6}$$

where n is the order of the system representation. In some situations it may be useful to consider the integral of $E(x)$ as an additional concept of the state space hyper-energy J, which divided by the length of interval $T=[t_0,t_1]$, defines a mean value of the $E(x)$.

III. THE STATE SPACE ENERGY FEEDBACK

In this part we try to attack the "problem of oscillations" not from the standard "observation of reality point of view", but from the opposite direction, i.e. we intend to develop a consistent approach to the real-world situations from a "generation of controlled oscillations point of view." The objective is to stabilize the state space energy $E(t)$ on any prescribed value E^* by means of a linear controller, but under the assumption that instead of the measured output signal $y(t)$, the information about the actual value of the state space energy $E[x(t)]$ is assumed to be available to the controller.

At least the following three interpretations are natural:

- either the state space energy is continuously measured, and a standard linear "output error" controller is used, where not the informational output $y(t\}$, but the integrated output dissipation power is used in the feedback informational channel [2], [3],
- or the actual state vector x(t) is continuously measured and used in the feedback informational channel; then the corresponding actual value of the state space energy is computed and a standard linear "output error" controller is used,
- or the actual values of the input $u(t)$ and that of the output $y(t)$ are continuously measured and used in the feedback informational channel, including a state reconstructor [3] and a state energy error controller.

The structure for single input-single output system with nonlinear part of controller is shown in the Fig.1.

The proportional-integral (PI) controller based on state space energy is shown in Fig. 2, where E^* is prescribed value of energy and x_i^2 is state space variable (the total state space energy is given by eq. (6)).

Let's start with analysis of the state representation eq. (1) where the information about the system structure is contained in the triple of matrices *(A, B, C),* e.g. as defined by eq. (2), where the *diagonal elements* of the matrix A represent the *dissipation parameters,* the *off-diagonal elements* of represent the *internal interaction parameters* between both the first order subsystems, and the *elements* of the matrices B and C represent the *parameters of external interactions.* Two typical solutions of the *state energy error control problem* are illustrated by simulation results: *harmonic oscillations* and *generation of chaotic oscillations.*

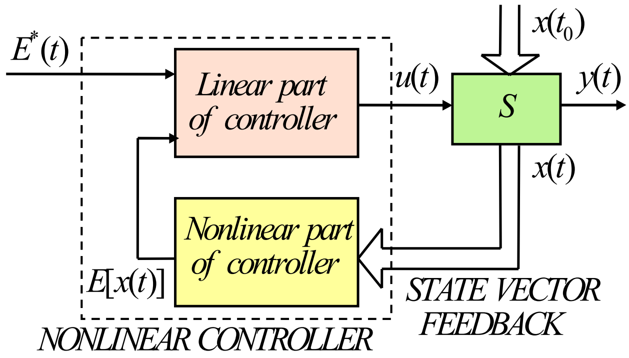

Fig.1. Linear system with nonlinear part of controller and the state vector measurement

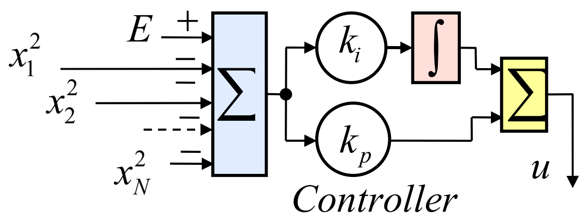

Fig. 2. Block diagram of PI controller based on state space energy control

The block diagram of linear quadrature oscillator with 2 dissipations is shown in Fig. 3 (dissipations are α_1, α_3).

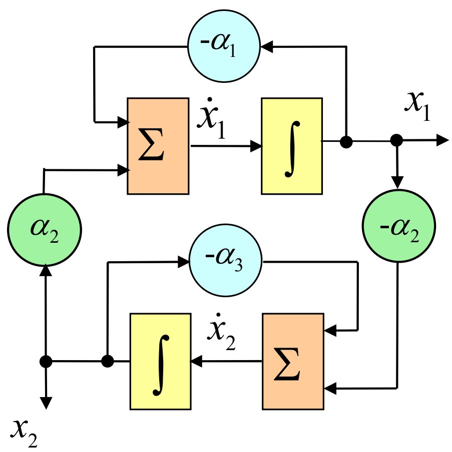

Fig. 3. Linear quadrature oscillator with dissipation parameters α_1, α_3. The frequency is controlled by parameter α_2.

This system can be described by as second order system with the dissipation α_1 α_3 and frequency proportional of α_2.

$$\begin{aligned} \dot{x}_1 &= -\alpha_1 x_1 + \alpha_2 x_2 \\ x_2 &= -\alpha_2 x_1 - \alpha_3 x_2 \end{aligned} \tag{7}$$

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Because of dissipativity, without control, the oscillation in this system vanishes after short time which depends on initial conditions and values of dissipative coefficient. Using of different controllers is possible for amplitude stabilization of oscillations [6, 7]. In this paper the new principle based on state space energy was selected. The block diagram of linear quadrature oscillator with proportional-integral controller is displayed in Fig. 4.

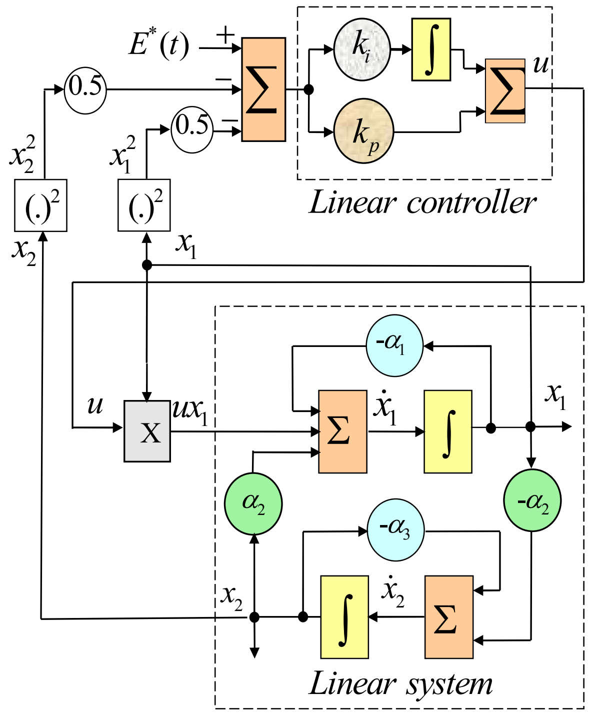

Fig. 4. The linear quadrature oscillator controlled by a state energy error PI-controller

The whole system - oscillator with PI controller with nonlinear feedback is represented by

$$
\begin{aligned}
&\dot{x}_1 = -\alpha_1 x_1 + \alpha_2 x_2 + x_1 u(t) \\
&x_2 = -\alpha_2 x_1 - \alpha_3 x_2 \\
&\dot{x}_3 = k_I \tilde{E}(t) \\
&\tilde{E}(t) = k_I \left(E^* - E(t) \right) \\
&E(t) = \tfrac{1}{2}\left(x_1^2 + x_2^2 \right) \\
&u(t) = x_1 \left[k_P \left(E^* - \tfrac{1}{2}(x_1^2 + x_2^2) \right) + x_3 \right]
\end{aligned}
\tag{8}
$$

The first equation can be rewritten as

$$\dot{x}_1 = x_1 (u(t) - \alpha_1) + \alpha_2 x_2 \tag{9}$$

From this equation can be seen that system can be dissipative if

$$u(t)-\alpha_1<0 \tag{10}$$

or anti-dissipative if

$$u(t)-\alpha_1>0 \tag{11}$$

therefore with appropriate control this system can hold desired energy. Based on previous results, the dissipativity/anti-dissipativity is controlled by controller which must hold prescribed energy E^* where state space energy of oscillator is given as

$$E[x(t)] = \frac{1}{2}(x_1^2 + x_2^2) \tag{12}$$

Results depend on proportional and integral gains of PI controller. It will show that for some gain values of PI controller the system can be chaotic but holds (in average) the prescribed energy. The system can be therefore simply switched as sinusoidal oscillator or system with chaotic oscillations.

IV. Results of Computer Simulations

The system according Fig. 4, described by eq. (8) was simulated (System 1) for different values of gains of PI controller.

On the first, the prescribed energy was $E_1^*=1.5$ (from time $t\in\langle 0$ to $150\rangle$) and $E_2^*=3$ (from time $t\in(150$ to $400\rangle$) with initial conditions $x_1(0)=0.1$; $x_2(0)=0$; $x_3(0)=0$ and $k_i=0.0015$; $k_p=0.3$; $\alpha_1=0.01$; $\alpha_2=1.4$; $\alpha_3=0.01$. For gain values of PI controller the system work as sinusoidal oscillator. The results are shown in Fig. 5 (phase portrait), Fig. 6 (time evolution of state variables), Fig. 7 (time evolution of state space energy) and Fig. 8 (frequency spectrum).

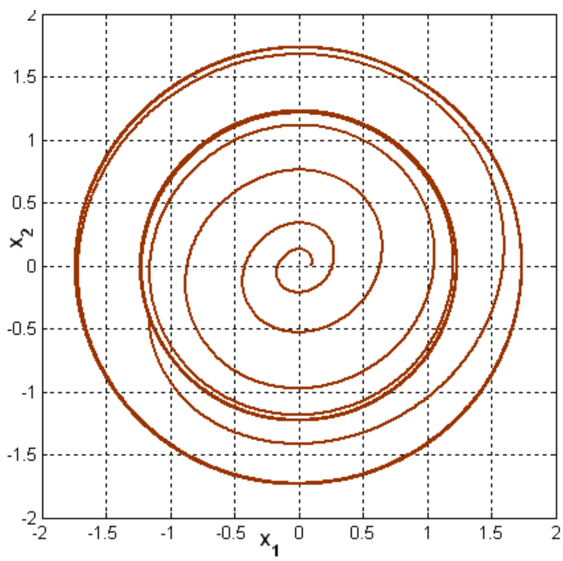

Fig. 5. Phase portrait of System 1 for $k_i=0.0015$; $k_p=0.3$; $\alpha_1=0.01$; $\alpha_2=1.4$; $\alpha_3=0.01$

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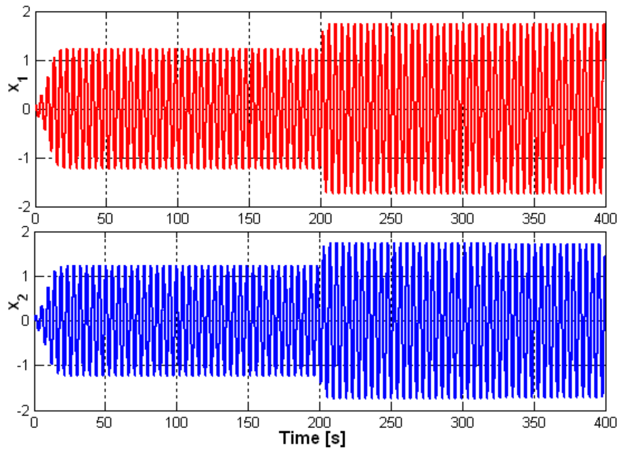

Fig. 6. Time evolution of state variables x_1 and x_2 for System 1 for k_i=0.0015; k_p=0.3; α_1=0.01; α_2=1.4; α_3=0.01

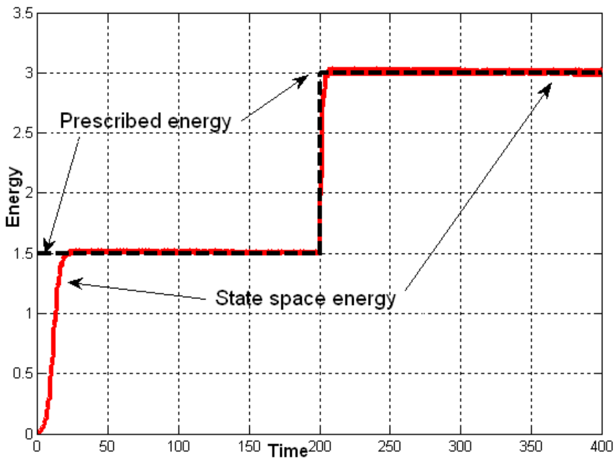

Fig. 7. Time evolution of the prescribed energy (dash line) and state space energy (solid line) of System 1 for k_i=0.0015; k_p=0.3; α_1=0.01; α_2=1.4; α_3=0.01

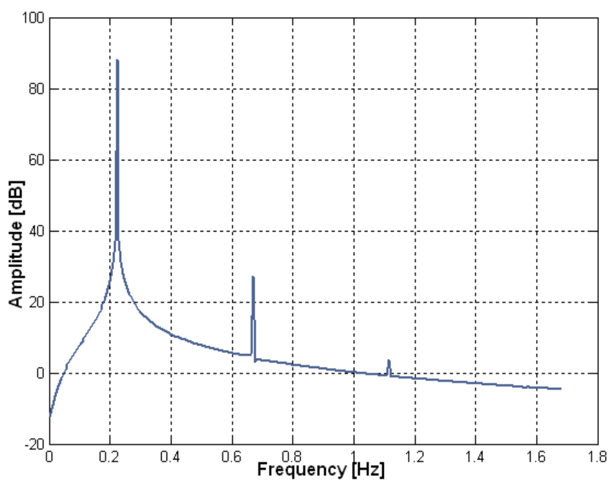

Fig. 8. The frequency spectrum of the state space variable x_1 of System 1 for k_i=0.0015; k_p=0.3; α_1=0.01; α_2=1.4; α_3=0.01

On the second, the prescribed energy was E_1^*=1.5 (from time $t\in\langle 0$ to $150\rangle$) and E_2^*=1.4 (from time $t\in(150$ to $300\rangle$) with initial conditions $x_1(0)$=0.1; $x_2(0)$=0; $x_3(0)$=0 and k_i=0.885; k_p=0.099; α_1=1; α_2=1.4; α_3=1.4. For this gain values of PI controller the system work as chaotic system. The results are shown in Fig. 9 (phase portrait), Fig. 10 (time evolution of state variables), Fig. 11 (time evolution of state space energy) and Fig. 12 (frequency spectrum) [8, 9, 10, 11].

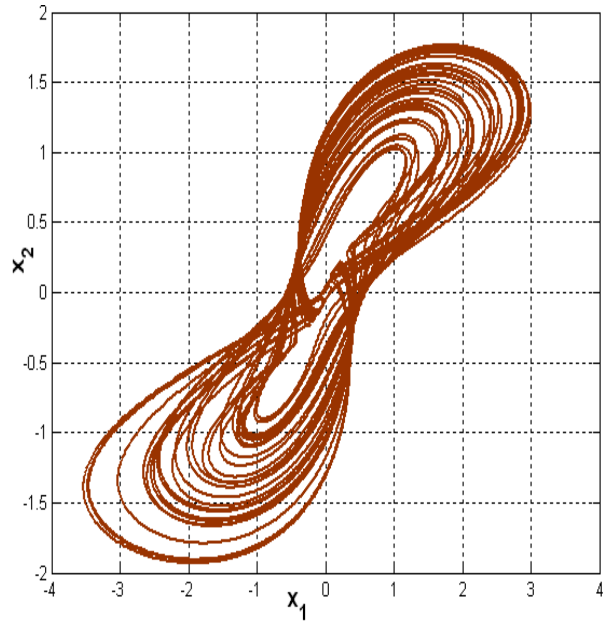

Fig. 9. . Phase portrait of System 1 for, k_i=0.885; k_p=0.099; α_1=1; α_2=1.4; α_3=1.4 and initial conditions $x_1(0)$=0.1; $x_2(0)$=0; $x_3(0)$=0

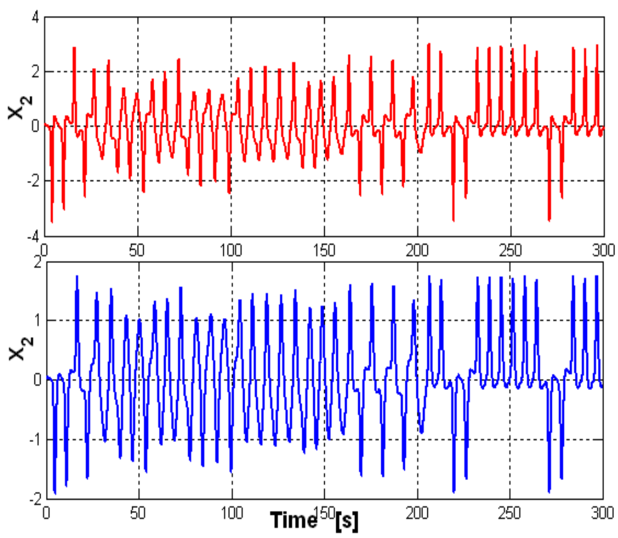

Fig. 10. Time evolution of state variables x_1 and x_2 for System 1 for k_i=0.885; k_p=0.099; α_1=1; α_2=1.4; α_3=1.4

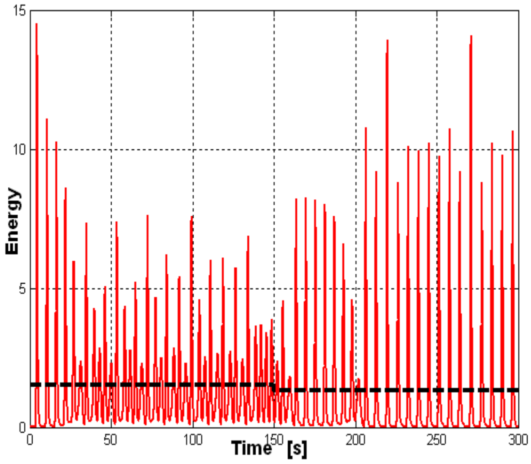

Fig. 11. Time evolution of the prescribed energy (dash line) and state space energy (solid line) of System 1 for k_i=0.885; k_p=0.099; α_1=1; α_2=1.4; α_3=1.4

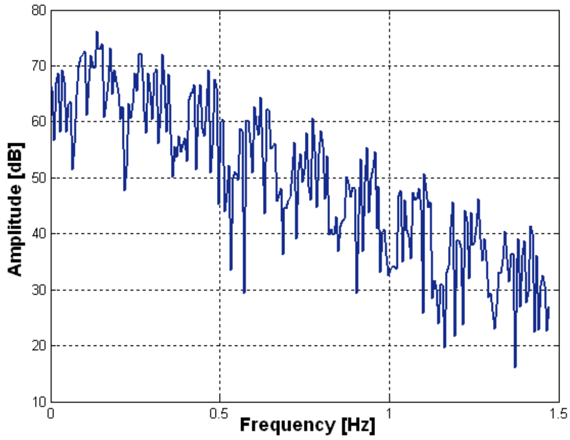

Fig. 12. The frequency spectrum of the state space variable x_1 of System 1 for for k_i=0.885; k_p=0.099; α_1=1; α_2=1.4; α_3=1.4

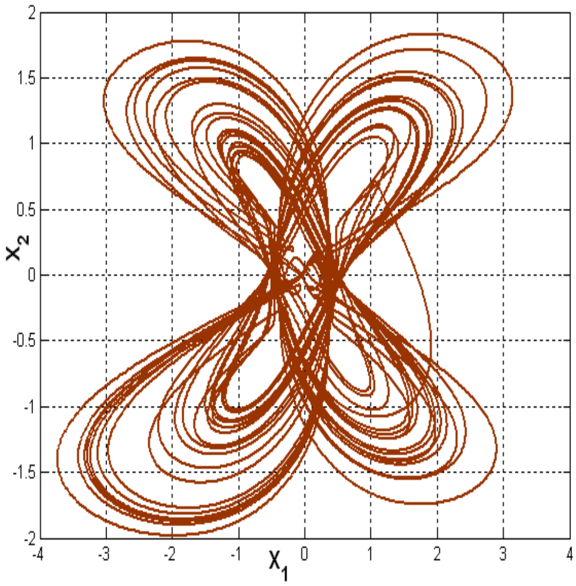

Fig. 13. Phase portrait of System 2 with reversed rotation, k_i=0.885; k_p=0.099; α_1=1; α_2=1.4; α_3=1.4.

On the third the same system was used, but the sign of 2 coefficients α_2 and -α_2 was swapped in time t=150, therefore "*rotation*" of the system was reversed. The simulation results leads to 4 wing chaotic system (System 2), see phase portrait in Fig. 13 and the next figures 14, 15, 16

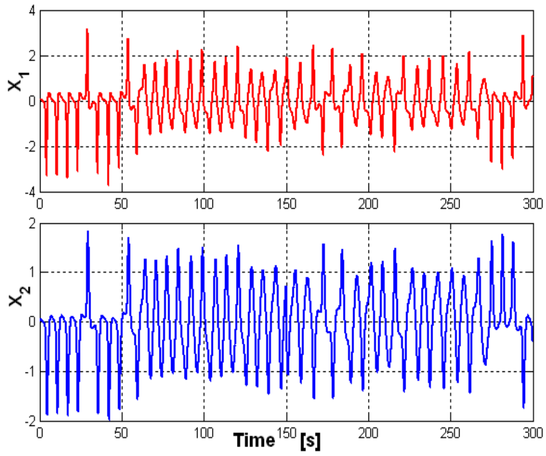

Fig. 14. Time evolution of system 2 with reversed rotation, k_i=0.885; k_p=0.099; α_1=1; α_2=1.4; α_3=1.4.

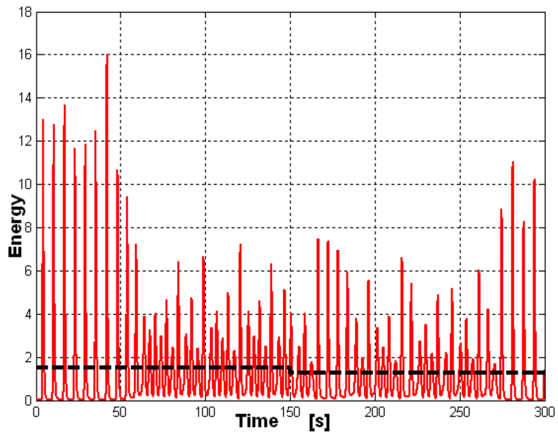

Fig. 15. The state space energy of system 2 with reversed rotation, k_i=0.885; k_p=0.099; α_1=1; α_2=1.4; α_3=1.4.

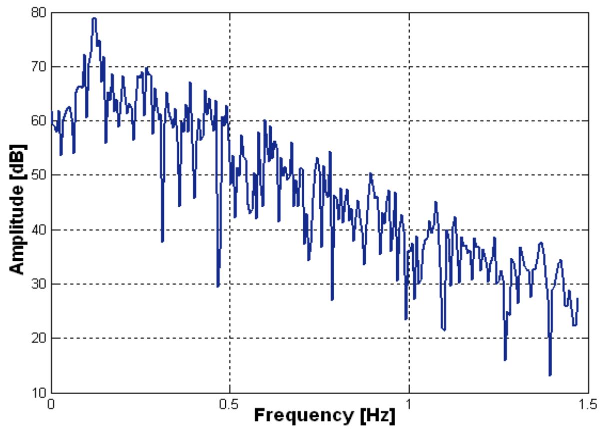

Fig. 16.The frequency spectrum of system 2 with reversed rotation, k_i=0.885; k_p=0.099; α_1=1; α_2=1.4; α_3=1.4.

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TABLE I. SYSTEMS PROPERTIES.

	System 1		System 2	
State variable	x_1	x_2	x_1	x_2
Lyap. Exponent	0.031	0.037	0.038	0.048
Hurst exponent	0.71	0.798	0.713	0.80
Capacity Dim.	1.32	1.29	1.36	1.27
Correl. Dim.	1.67	1.71	1.66	1.56

In Table I some important characteristic of the booth chaotic systems (System1 and 2) are presented (calculated from state variables x_1 and x_2):

Largest Lyapunov exponent

Hurst exponent

Capacity dimension

Correlation dimension.

CONCLUSION

In this paper the several types of feedback system based on linear controlled system, linear controller but nonlinear state space feedback was presented and simulated. The theory of state space energy approach was used. Depending on parameters of the controller the system can generate sinusoidal, non sinusoidal or even chaotic signal.

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Optimization of Pacemaker Leads Place Based on Vectorcardiography Signal Processing

M. Stork, V. Vancura

***Abstract* —** A pacemaker is a small electronic device implanted under the skin near the collarbone. Pacemakers monitor the heart's electrical activity. If the heart is beating too slowly or pausing too long between beats, the pacemaker will provide electrical impulses that stimulate the heart to beat. The pacemaker itself consists of a small box (the pulse generator with battery) and usually two leads that are placed in the heart and most important are right places of leads tips. This paper is devoted to system and software which can support physician find almost optimal place of pacemaker lead's tips in heart. Results will be helpful for prolonging battery longevity and reducing the stimuli pain on patients with implantable medical devices..

***Keywords*—**3-D ECG, heart, pacemaker, perimeter, resynchronization, stimulation, vectorcardiography.

I. Introduction

THE pacemaker is a device which takes over the timing control of the ventricular contraction from the body's natural system to ensure a rate fast enough to allow an active life for the patient. Pacemakers basically consist of a battery, a timing device and electrodes. The battery must be capable of supplying enough current to stimulate or excite the muscles in the ventricles and perhaps the atria for a number of years. Usually 4 to 6 volt pulses are used to excite the heart with duration of between 1.5 and 2.5 milliseconds. The electrical connection is made from the pacemaker to the patient's heart by leads, see Fig. 1. The electrodes are either implanted in the heart or stitched to the surface of the heart. As a temporary measure, electrodes may be floated into the ventricles of the heart in the same way as a catheter is introduced during blood pressure measurement.

The increasing prevalence of devices specifically designed to improve timings within the cardiac cycle (i.e. cardiac resynchronization therapy) has created a clinical need to accurately monitor the effects on cardiac performance of changes to pacing configurations. Optimization of pacemaker atrioventricular (AV) and interventricular delay settings for individual patients maximizes the hemodynamic benefit of pacing [1–4] and might be approached by monitoring stroke volume or BP, while changes are made to the settings. The most widely used quantitative approach for pacemaker optimization uses echocardiography to measure cardiac output using Doppler; however, this is time consuming, relies on experienced operators, and has limited reproducibility [3].

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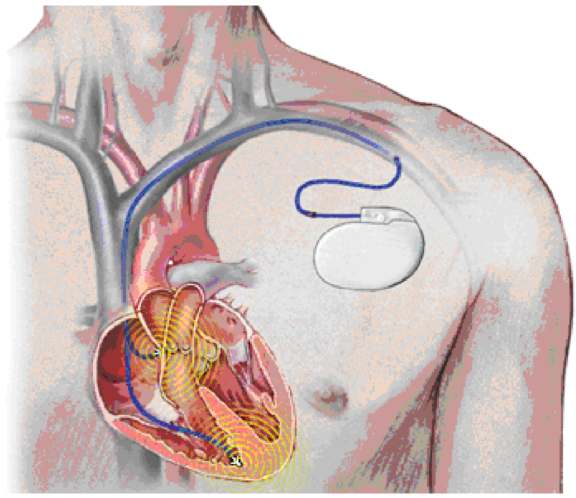

Fig. 1. The body, heart, pacemaker (Pace) and pacemaker leads situation

II. Methods

For AV optimization of cardiac resynchronization therapy (CRT) in this paper is based on evaluation of vectorcardiographic signal. For the signal acquisition from the patient, the non-invasive system CARTO is used for the reconstruction of map.12-electrodes are applied to the patient's torso and connected to the non-invasive imaging system and surface potentials are recorded [4, 5, 6]. The 3D epicardial bicameral (atria or/and ventricles) geometries are reconstructed from segmental CT images. The relative positions of body surface electrodes can be visualized on the torso geometry. The system reconstructs epicardial potentials, unipolar electrograms, and activation maps from torso potentials [7 - 12].

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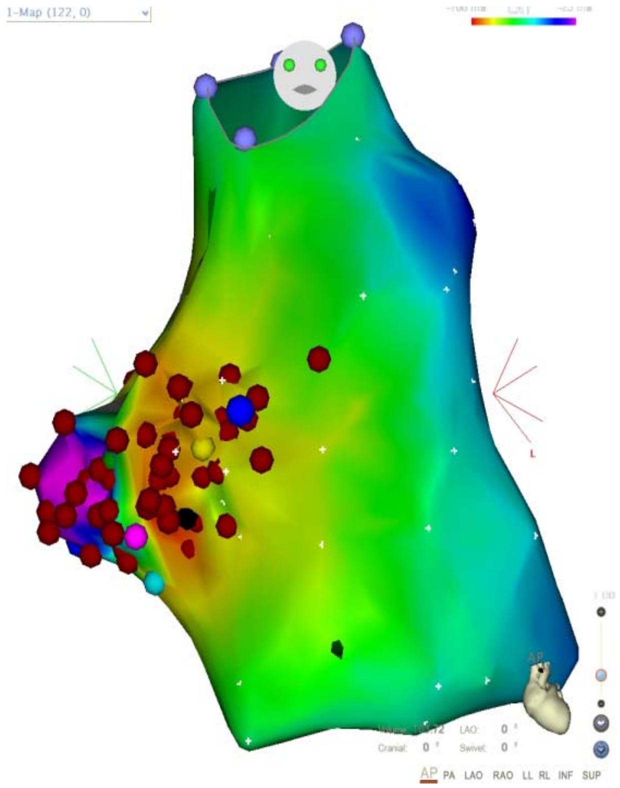

Fig. 2. The example of 3-dimensional map of heart of the patient

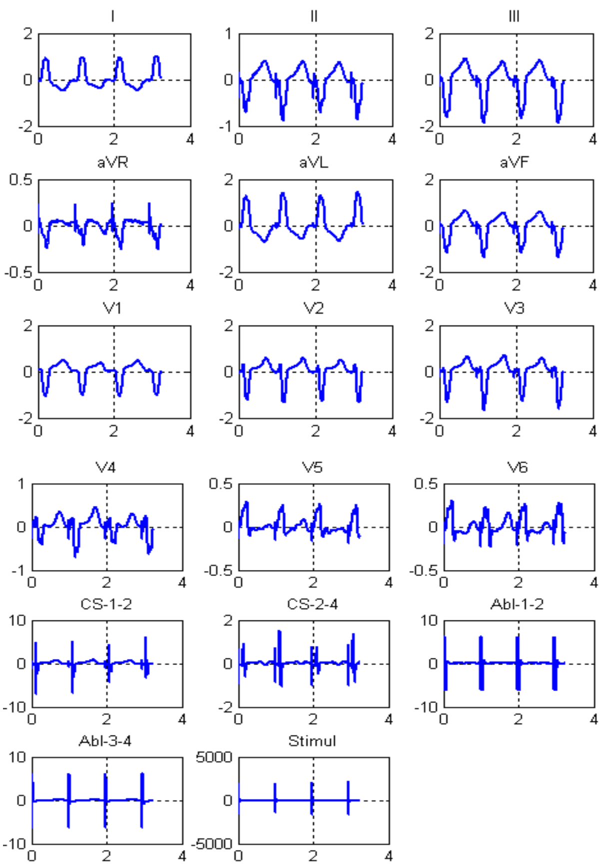

Fig. 3. The example of ECG and stimulation signals of the patient for one point of heart map (see Fig. 2)

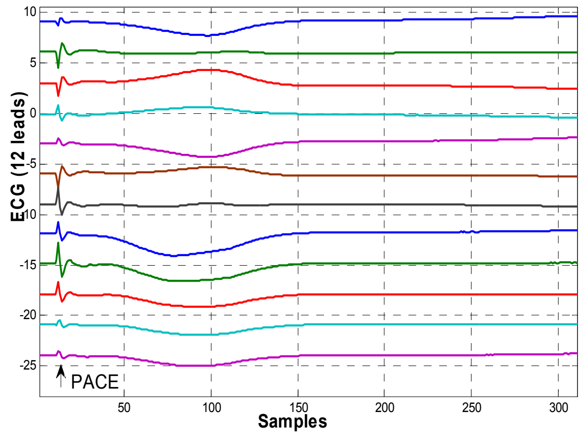

Fig. 4. The one period of raw 12 leads ECG signals with pacemaker stimulation pulses (signed as PACE).

The example 3-dimensional map of patient is shown in Fig. 2. The small circles are successive positions of catheter. For each of this position the 12 leads ECG signals were measured sampled and stored in memory (together with stimulation signals) of the personal computer (PC). The example is shown in Fig. 3.

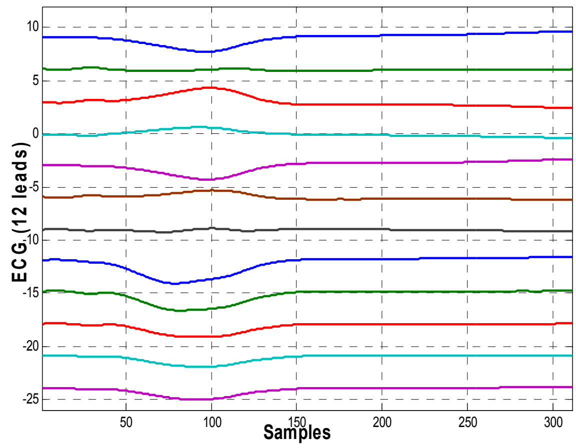

Fig. 5. The 12 leads ECG signals (from Fig. 4) after filtration by 6-th order Butterworth filter. The stimulation pulses from pacemaker are removed

From 12 leads ECG signals the one period is taken for next processing. Raw signal (without filtration) is displayed in Fig. 4. This signal is filtered by 6-th order Butterworth filter for stimulation pulses suppression. The filtered signal is presented in Fig. 5. From filtered signals the 3 dimensional ECG signal is calculated

$$\begin{bmatrix} X \\ Y \\ Z \end{bmatrix} = D^{-1} \begin{bmatrix} V_1 \\ \vdots \\ V_6 \\ I \\ II \end{bmatrix} \qquad (1)$$

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where D is Dower matrix [5]

$$D^{-1} = \begin{pmatrix} -0.172 & -0.073 & 0.122 & 0.231 & 0.239 & 0.193 & 0.156 & -0.009 \\ 0.057 & -0.019 & -0.106 & -0.022 & 0.040 & 0.048 & -0.227 & 0.886 \\ -0.228 & -0.310 & -0.245 & -0.063 & 0.054 & 0.108 & 0.021 & 0.102 \end{pmatrix} \quad (2)$$

The example of 3-D ECG signal calculated by (1) is shown in Fig. 6 and signal area in Fig. 7.

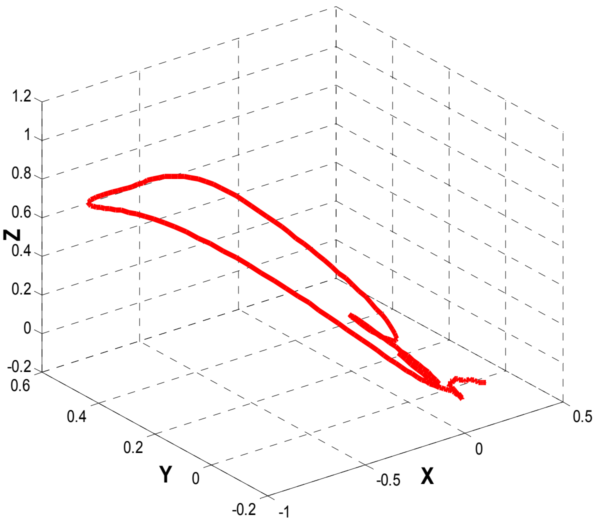

Fig. 6. The example 3-D ECG calculated by (1)

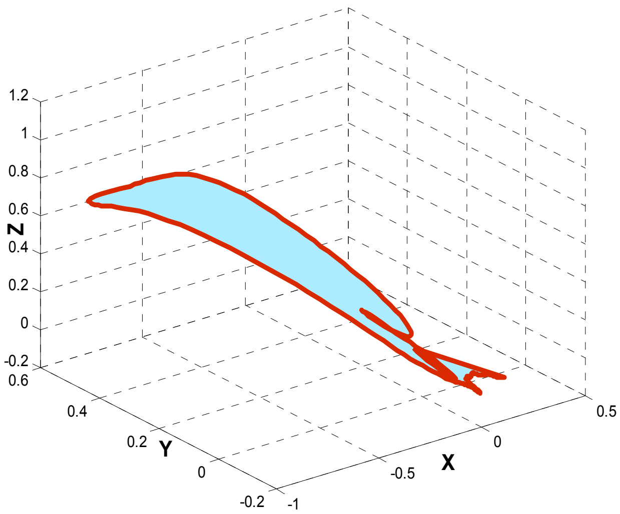

Fig. 7. The area and perimeter (L=4.11) of 3 D-ECG signal.

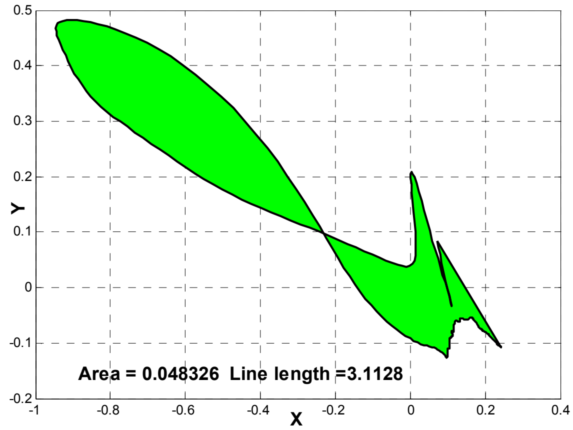

Fig. 8. The projection of 3-D ECG signal to 2-D XY area

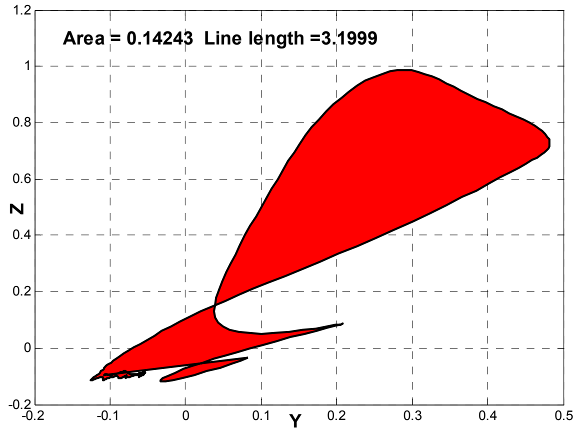

Fig. 9. The projection of 3-D ECG signal to 2D YZ area

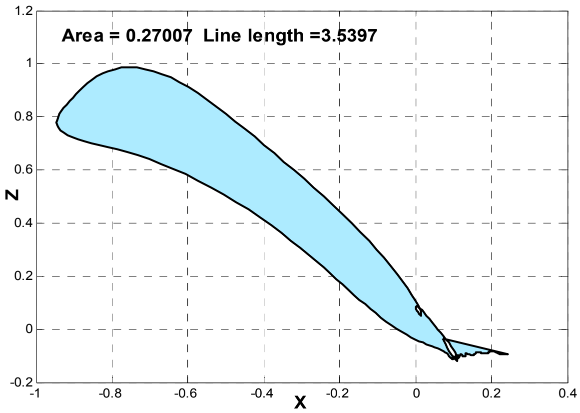

Fig. 10. The projection of 3 D-ECG signal to 2D XZ area

III. Results

The previous approach was used for evaluation of ECG signal by means of "area". The projection of 3-D signal (Fig. 7) on separate areas of XY, YZ and XZ is shown in Fig. 8 (projection XY), Fig. 9 (projection YZ) and Fig. 10 (projection YZ). In Fig. 8 – 10, the area and length of the line for 1 period of filtered ECG (stimulation pulses are removed) is presented in Tab. I.

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TABLE I. AREA AND LENGTH OF PERIMETER FOR PROJECTION ECG IN XY, YZ AND XZ

Projectio n	Area	Perimeter length
XY	0.05	3.1
YZ	0.14	3.2
XZ	0.27	3.5

From previous results can be seen, that area is changed more rapidly than lengths of the ECG perimeter. The lengths of perimeter for 3 dimensional ECG signals for 10 patients are shown in Tab. II. The patient's No. 2 and 5 are out of mean value (approx. 4±0.6 for normalized 1 period of 3-D ECG) and amplitude of stimulation pulse (generated by pacemaker) or place of PACE electrodes in heart can be changed for optimal function.

TABLE II. LENGTH OF PERIMETR OF 3 D-ECG (FOR 10 PATIENTS)

Patient No.	Perimete r
1	4.07
2	**→ 8.50**
3	3.68
4	4.00
5	**→ 6.56**
6	4.11
7	3.65
8	4.57
9	3.58
10	5.52

According to the experimental results, the optimization of pacemaker's pulse or pacemakers leads places in heart can be recommended. From result of the study (so fare only 10 patients with pacemakers) can be shown, that areas of ECG and 3-D ECG perimeter lengths probably has some almost optimal value. The physician can changed places of pacemaker's leads, amplitudes of pulses or delay for optimal function.

IV. CONCLUSION

In this paper, the evaluation system based on ECG signal processing was described. The method is based on 3 dimensional ECG projections in three 2 dimensional planes, area of the projections and length of 3-D ECG perimeter are evaluated by software. Using this system and software, the physician can find optimal values of pacemaker's pulses and thus reduce the energy consumption of such a pacemaker, its longer function, etc. So fare sufficient number of patent was not tested, therefore further studies are necessary to validate this approach.

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A 12bits 40MSPS SAR ADC with a redundancy algorithm and digital calibration for the ATLAS-LArg calorimeter readout

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***Abstract*—**This paper presents a SAR ADC with a generalized redundant search algorithm offering the flexibility to relax the requirements on the DAC settling time and allowing a digital calibration, based on a code density analysis, to compensate the capacitors mismatching effects. The proposed architecture uses a DAC with only 2^{N-1} unit capacitors, for N-bit resolution, and a simplified monotonic switching algorithm. The design is fully differential featuring 12-bit 40MS/s in 130-nm 1P8M CMOS process.

***Keywords*—**Digital calibration, Non-binary, Redundancy, SAR ADC, Switching algorithm.

I. INTRODUCTION

Particle detectors, such as liquid argon (LArg) calorimeter used in ATLAS experiment at the LHC (Large Hadron Collider), generate very large dynamic signals which require a sophisticated front-end electronics. This readout includes the noise optimization stages (low noise preamplifier, and analog multigrain filters), but one critical element is the Analog to Digital Converter (ADC). The requirements for our converter are 40MS/s at 12bits resolution. In this configuration pipeline architecture was widely used during this last years. But following the scaling of CMOS process, Successive Approximation Register (SAR) architecture appears to be more suitable in term of power dissipation. In this paper, a redundant SAR ADC is proposed, to achieve the high resolution required despite the capacitors mismatching. The paper is organized as follows. In Section II, the conventional SAR ADC is reviewed. Section III introduces the generalized non-binary search algorithm. Section IV presents the proposed redundant SAR ADC. In Section V, the design's simulations results are discussed.

II. CONVENTIONAL SAR ADC

Recently, SAR ADCs have been widely used for high-resolution, medium sampling rate, and low-power applications [1]. SAR ADCs are actually known to achieve very low power consumption owing to the extensive use of switching capacitor based circuits.

A SAR ADC is composed of a Sample and Hold S/H circuit, a comparator, a DAC, and a Successive Approximation Register logic circuit as shown in (Fig. 1): The analog input signal (V_{in}) is sampled by the S/H and compared with successive feedback voltage values (V_{DAC}) generated by the return DAC which is itself driven by a SAR algorithm designed to minimize the error between V_{in} and V_{DAC}. N clock periods are required to resolve the N digital output bits. To execute this procedure, the conventional SAR ADCs uses a binary search algorithm following a binary-weighted capacitive DAC which is used also to perform the sample-and hold function [2].

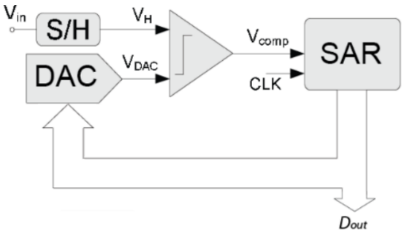

Fig. 1. Bloc diagram of a SAR ADC.

The drawback of the binary search algorithm is that it makes the ADC sensitive to decision errors due to capacitor matching limitations, incomplete DAC settling, parasitic capacitors, switch charge injections etc. Actually in case of an intermediate wrong decision, the following digitization process cannot recover, in Fig.2 the first comparison is wrong and this moves away V_{DAC} from V_{in}, which results in an error at the end of the conversion. Therefore one may guaranty an accuracy of quite 0.5LSB at each step of the SAR ADC processing. 12bits resolution for instance could not be achievable unless a big effort on matching is made for standard CMOS process.

We have created a Matlab model to evaluate just the capacitor matching limitations effects on a 12bits SAR-ADC. Simulation results are shown in Fig.3.

Fig. 2. Example of decision error due to incomplete DAC settling.

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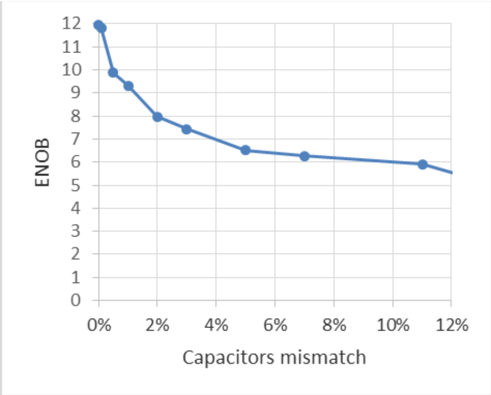

Fig. 3. Matlab simulations results for capacitors mismatch limitations on a 12 bits SAR ADC.

The pure binary search algorithm requires a strict and monotonic DAC section which is hard to combine with high density of integration that dramatically impacts the capacitor matching performances. To overcome these limitations, one solution is to move from the conventional binary search algorithm to a non-binary one.

III. Generalized Non-Binary Search Algorithm

A non-binary search algorithm makes the SAR ADC tolerant towards incomplete DAC settling errors, and it makes possible a digital correction algorithm that corrects the capacitor mismatch errors, which is identified to be the main limiting factor for 12bits resolution ADCs and higher.

By using overlapped search ranges (redundancy), the non-binary search algorithm, compensates the comparison decision errors made in earlier conversion steps as long as the error made is within a certain tolerance range. To achieve an N-bit resolution using a redundant search algorithm, the SAR ADC requires M comparison steps (M>N) to determines the output digital bits, the idea is to have 2^M possible comparison combinations and 2^N possible digital output combinations, and since M>N, therefore $2^M>2^N$. In other words, for a given output level D_{out}, there can be multiple comparison patterns leading to the same final result. Thus even if it happens for a comparison decision to be wrong, there is nevertheless a room for recovering a correct ADC output codes after the following steps. Fig. 4 illustrates an example of a 4-bit SAR ADC using 5-redundant steps.

Although, redundant search algorithm adds extra clock cycles to the conversion phase, the duration of these conversion steps can be made shorter (incomplete DAC settling) [4] and the overall conversion speed is then saved.

A SAR ADC implementing the non-binary search algorithm can use radix $r=2^{N/M}$ such as presented in [4] and [5]. An alternative method called *"a generalized non-binary search algorithm"* has been presented in [3] without restricting to radix of $2^{N/M}$. In each step *(k)* of conversion, to define the *k-th* bit, the analog input voltage is compared to a reference voltage (*Vref(k)*) generated according to a redundancy vector *p*.

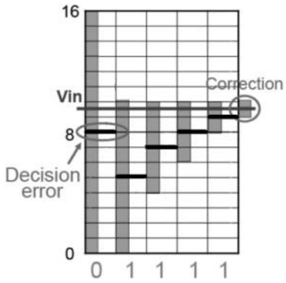

Fig. 4. Operation of a redundant search algorithm of a 4-bit 5-step SAR ADC.

Table-1 shows an example of the values of the redundancy vector *p* and the vector, of the acceptable errors, *q* in each step of conversion for a 12-bit 14-step SAR ADC.

TABLE I. A 12-BIT 14-STEP SAR ADC *P(K)* AND *Q(K)* VALUES

	Generalized non-binary search algorithm	
Step *k*	***p(k)***	***q(k)***
1	2048	24
2	1012	124
3	456	76
4	252	40
5	144	24
6	80	12
7	46	6
8	26	4
9	14	2
10	8	2
11	4	2
12	2	0
13	2	0
14	1	0

IV. Proposed Architecture

To implement the generalized non-binary search algorithm for an N-bit conversion, based on a M-step redundant SAR ADC, a series of corresponding reference voltage must be generated and next been compared to the incoming voltage signal. In other words the ADC must perform the additions/subtractions, between *Vref(k-1)* and *p(k)*. For these operations a digital architecture approach is possible [3], but this strategy comes with an increase of the overall complexity of the design, and some extra delay and power consumption in the digital part of the ADC. Another approach is to perform the operations in the analog domain by using the DAC [6]. Each value of *p(k)* is then stored in capacitor's values. This strategy presents the advantage of a reduced and simplified digital part of the circuit, which leads to reduced power consumption, compared to the one proposed in [3].

In this paper, we propose a fully differential N-bit M-step redundant architecture that implements the generalized non-binary search algorithm in the analog domain, a new structure is designed so as to only use 2^{N-1} unit capacitors in the DAC instead of 2^N in conventional solutions. This allows reducing the dynamic power consumption as well as the total capacitance

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compared to the architecture proposed in [6]. Fig.5 shows the proposed architecture.

During the sampling phase, the differential input signal (V_{in+} and V_{in-} respectively) are stored on the capacitors array. After this phase, in each step, the ADC compares the input signal with the corresponding *Vref(k)* generated, by switching the corresponding capacitor, following the switching algorithm explained hereafter. The DAC is not segmented in order to perform a good linearity and avoid the limitations associated with split-capacitor structure such as the parasitic capacitance at the sub-DAC output and the fractional value of the bridge capacitor.

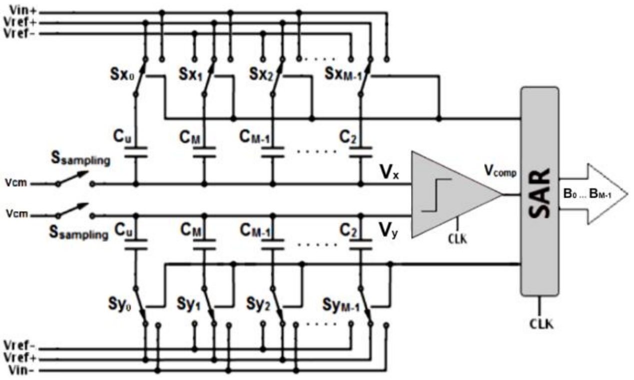

Fig. 5. The proposed N-bit M-step SAR ADC architecture (where $C_k=p(k)*C_u$ and $k = 2, 3. . . M$).

The high speed low noise comparator is implemented by using a multi-stage differential pair as shown in Fig.6.

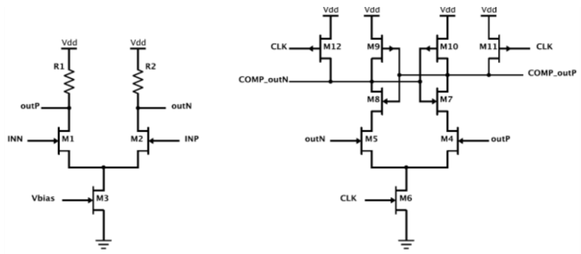

Fig. 6. Multistage comparator.

A. Proposed switching algorithm

The proposed redundant SAR ADC uses a simplified monotonic switching algorithm (see Fig. 7) which requires much less dynamic power consumption compared to the conventional switching algorithm.

One may notice that there is no switch-back operations and over the whole ADC, only one capacitor, is switched at each bit-cycle step, providing inherent immunity to the skew of the switch signals. At the end of the conversion, the N-bit digital output is calculated from the M-bit data. This proposed switching algorithm is also valid for the SAR ADC using the binary search algorithm, when $N=M$ and $C_k=2^{N-k}*C_u$; $2\le k\le N$.

B. Digital Calibration

The digital calibration used with our ADC is based on [7], it uses the original ADC core without adding any extra analog hardware on-chip or any additional reference channel in the design, and it is based on a statistical approach that uses a code density measurements to estimate the actual step sizes which map accurately the M-bit output into a final N-bit digitalized output.

In our case, a calibration signal is used to simplify the calibration algorithm presented in [7], during the calibration phase a full-scale ramp is sent to the ADC input to create a histogram of the 2^M possible output codes, after having normalized this histogram for the number of samples, an equation associated with each code bin is formulated, then an equations system is obtained by subtracting the neighboring equations. To calculate the estimated value of the step sizes the algorithm searches for a solution in this equations system.

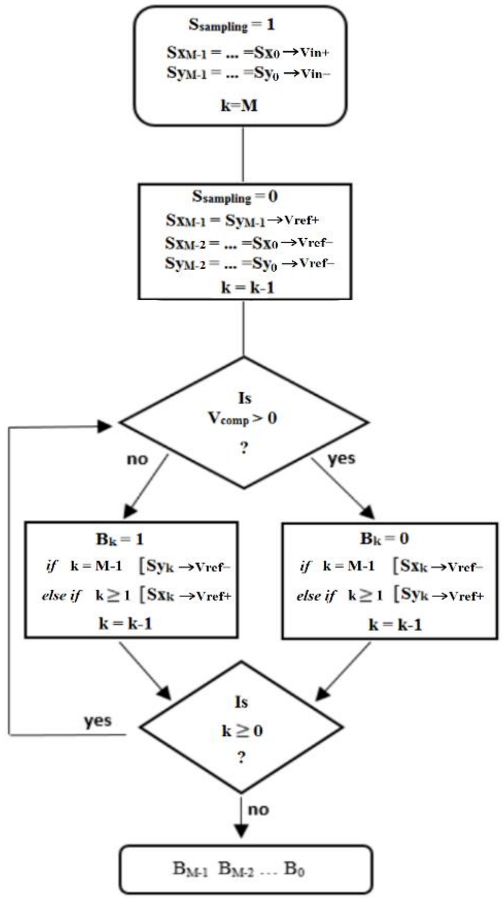

Fig. 7. Switching algorithm for the proposed SAR ADC.

V. Simulation Results

Using the proposed architecture and the coefficients of Table.1, we designed in the 130-nm 1P8M IBM CMOS a fully differential 12bits redundant SAR ADC working at 40MSPS with a $2V_{pp}$ full-scale input range. Fig. 8 shows the layout of the redundant SAR-ADC designed and submitted to MOSIS run. The power consumption of the core ADC is about 25mW from a 1.5V supply.

Fig.9 shows the simulation results for the successive DAC approximation signal at the comparator input. In Fig.9 (a) all settlings are complete, therefore the ADC performs the conversion without any decision error, and the D_{out} calculated

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from the 14bits is 3031. But in the configuration of Fig.9 (b) a wrong decision has been made in the second step due to an incomplete settling. However one can see how the ADC is capable to recover in the following steps, and D_{out} obtained finally is the same as in Fig.9 (a) (case without error). This illustrates the robustness of our redundancy architecture.

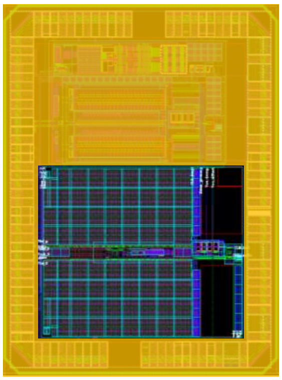
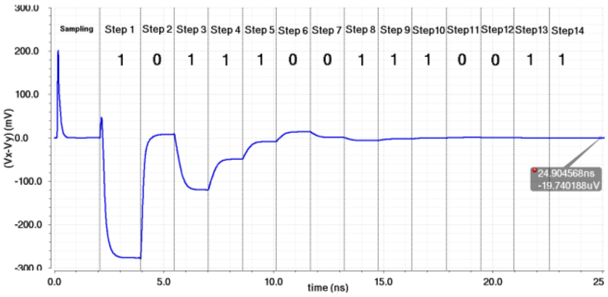


Fig. 8. The layout of the redundant SAR-ADC 12bit.



(a) Complete settling

(b) Incomplete settling in the first step

Fig. 9. The simulated DAC outputs voltage difference (Vx-Vy) of the proposed redundant architecture.

To evaluate the digital calibration regarding capacitor mismatching, a 5% capacitors mismatch error was inserted in the DAC and a 1.0546875MHz full-scale sine wave input was converted at 40-MSPS with 4096 samples, to simulate the static and dynamic performance. Fig. 10 and Fig. 11 show respectively the simulated INL and dynamic performance without and with calibration. Without calibration the maximum INL errors are +56.5/-56.8LSB and the ADC achieves 38.25dB of SNR, 40.53dB of SFDR and 5.56b ENOB. After calibration the maximum INL errors is reduced to +1.6/-1.7LSB and the ADC achieves 69.54dB of SNR, 64.23dB of SFDR and 11.15b ENOB.

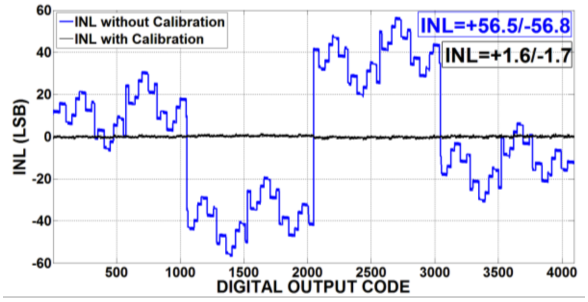


Fig. 10. The simulated INL without and with calibration.

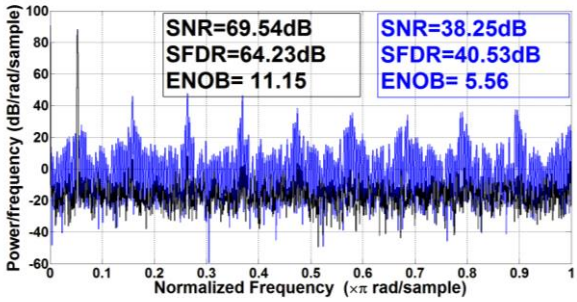


Fig. 11. The simulated FFT spectrum without and with calibration.

VI. Conclusion

A redundant SAR ADC has been presented with an efficient switching algorithm, and a digital calibration algorithm. The design of a generalized non-binary search algorithm is explained. Compared to previous works, this architecture presents the advantage of simplicity and minimizes the value of total capacitance. A design of a 12bits, 40MS/s configuration and its simulation results confirm the robustness of the proposed structure.

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On/Off Ratio Tuning of Schottky Barrier CNTFETs Based on Quantum Simulation Approach

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Abstract— Carbon nanotube field effect transistor (CNTFET) is one of the novel nanoelectronic devices that overcome those MOSFETs limitations. In this paper we have studied the effect of scaling of Schottky Barrier CNTFET (SB_CNTFET) insulator thickness (tox), high k dielectric materials, Gate length (L_G), L_G/tox Ratio and Schottky Barrier height on current-voltage characteristics of SB_CNTFET. The device metrics such as drive current (Ion), leakage current (Ioff) and Ion/Ioff ratio studied in this paper. The simulation results show the Ion/Ioff Ratio decreased with using Low k dielectric materials, Gate length (L_G<15nm & L_G>40nm), L_G/tox Ratio (Less than 18), too with increasing the insulator thickness and Schottky Barrier height.

Keywords: Carbon Nanotubes, SBCNTFET, Quantum Modeling.

I. Introduction

Today, two major types of CNTFETs have been introduced: Schottky barrier CNTFETs (SB_CNTFETs) and MOSFET like CNTFETs (MOSCNTs). SB_CNTFETs are made by contacting an intrinsic CNT to the metal electrodes. In SB_CNTFETs the dominant mechanism of delivering current is tunneling through Schottky barriers at the source and drain junctions[1].

MOSCNTs have higher on and lower off currents than SB_CNTFETs and behave like normal MOSFETs because in these transistors the Schottky barriers' width at the source and drain contacts and thus the ambipolar conduction have been suppressed[2]. The dominant mechanism of delivering current in such transistors is the thermionic emission which is controlled by modulating the barrier in the intrinsic region of the channel by using appropriate gate voltages. However in this case, tunneling of the electrons from valence band to the conduction band and vice versa constitutes a leakage current that increases the total current in high reverse gate voltages and prevents MOSCNTs from being unipolar perfectly. In this paper we suggest schottky barrier profile for the source and drain terminals. In this work, a SB_CNTFET will be studied for obtaining a high on/off current ratio.

II. SB-CNTFET

The transistor is coaxially-gated because this structure provides the best controlling state on channel by gate field, and consequently the minimum length of channel is needed[3]. The schematic of this device is represented in Fig. 1.

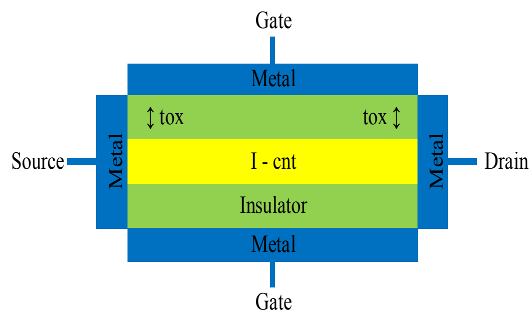

Fig. 1. Cross-sectional view of the device, (8, 0) zigzag CNT, length across the device = 20 nm, gate insulator dielectric constant (κ) = 16, gate insulator thickness (tox) = 1.5 nm.

Here, the on/off current ratio (Ion/Ioff) based on gate parameters is investigated. We justify the obtained results in detail with respect to I_{DS} vs. V_{GS} of the device.

A. Current mechanisms

Knowing the current mechanisms in a SB-CNTFET makes it easier to understand the changes in performance based on variations in device's parameters[3]. Figures 2(a) and 2(b) illustrate the Electron distribution function on energy band diagram trends with respect to changes in gate and drain fields, respectively, whereas the source is taken as the reference.

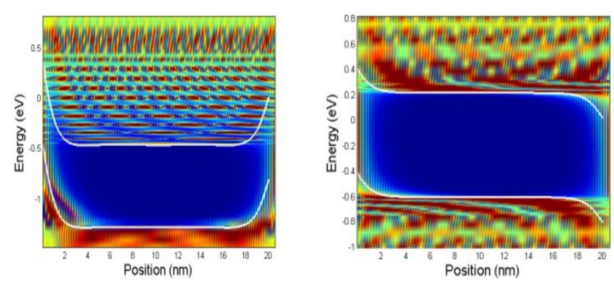

Fig. 2. Electron distribution function on energy band diagram of the device with the same conditions as in Fig. 1 at T = 300 K and VD = 0.4 V: (a) VG = 0.4 V, (b) VG = 1 V. The inset shows the simple tunneling states created in channel valence band.

III. Simulation and Results

Using the described semi-classical model, the current of the SB_CNTFET has been calculated and the dependence of its magnitude on the bias voltages has been investigated. The source contact is assumed to be ground.

Figures 3 and 4 displays the current-voltage curve and on/off ratio variations, their plotted against the gate length variation and as indicated, as the length become less than

15nm (L_G<*15nm*) or the gate length become greater 40nm (L_G>*40nm*), the on/off currents will be reduced substantially.

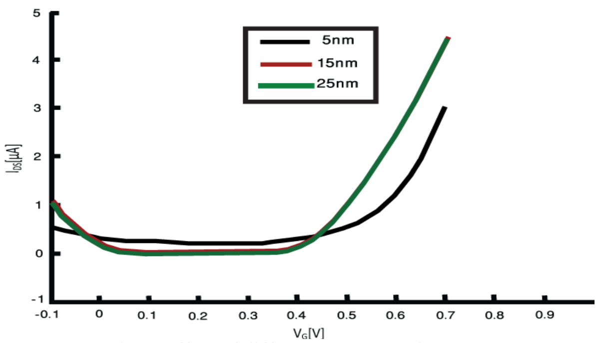

Fig.3. Effect of different Gate Length on I_{DS} vs. V_{GS}.

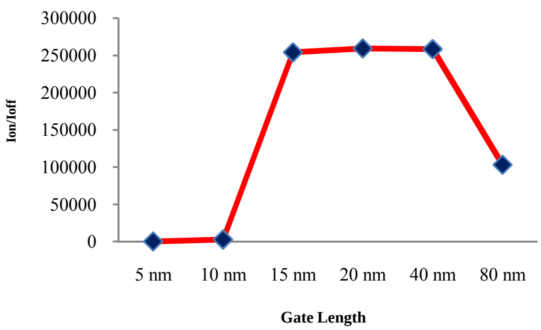

Fig. 4. Ion/Ioff ratio vs Gate Length.

Figure 5 displays the current-voltage curve and on/off ratio variations, their plotted against the gate insulator thickness variation and as indicated, as the thickness increases, the on/off currents will be reduced substantially.

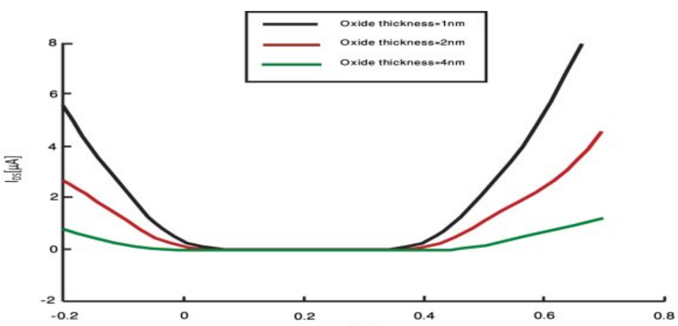

Fig.5. Effect of different oxide thickness on I_{DS} vs. V_{GS}.

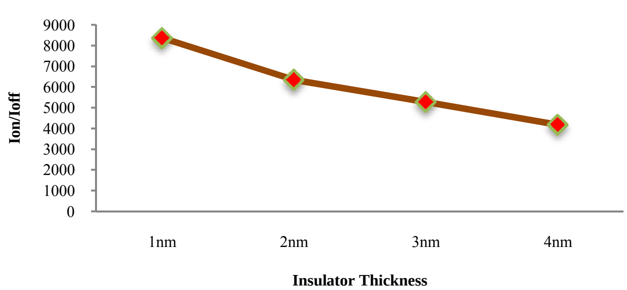

Fig. 6. Ion/Ioff ratio vs oxide thickness for transistor with the same.

Figure 7 displays the current-voltage curve of SB-CNTFET based on different constants of prepared materials and figure 8 shows the variation of the on/off current ratio against material types for gate insulator and as indicated, using the materials with high dielectric constants increases the on current and the on/off current ratio will become high.

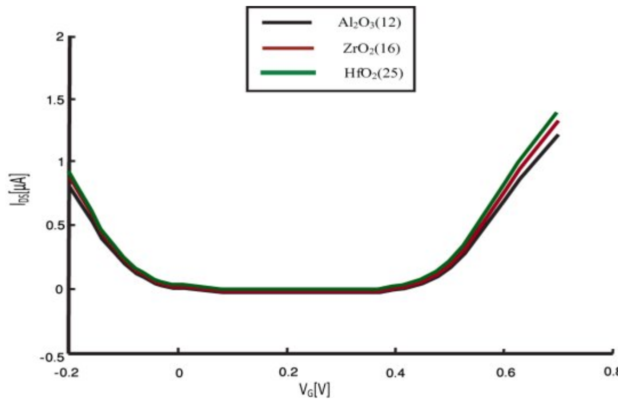

Fig.7. Effect of different dielectric materials on I_{DS} vs. V_{GS}.

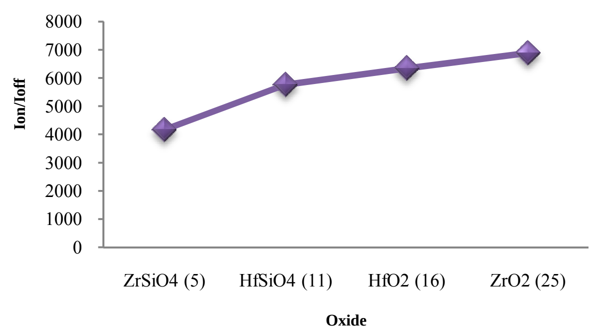

Fig. 9. Ion/Ioff ratio vs. dielectric materials.

Its Empirically investigated, if the L_G/tox Ratio becomes lower than 18, so the on/off ratio will be reduced substantially.

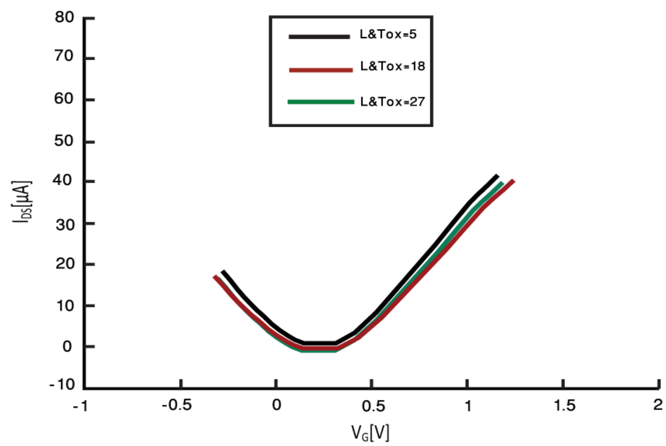

Fig. 10. Effect of different L_G/tox Ratio on I_{DS} vs. V_{GS}.

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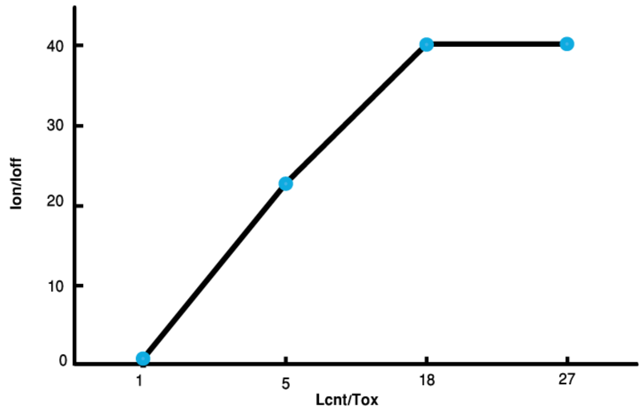

Fig. 11. Ion/Ioff ratio vs L_G/tox Ratio

At the final stage, its clear if the schottky barrier height increased, because of tunneling the electrons and holes, the on/off ratio will be decreased.

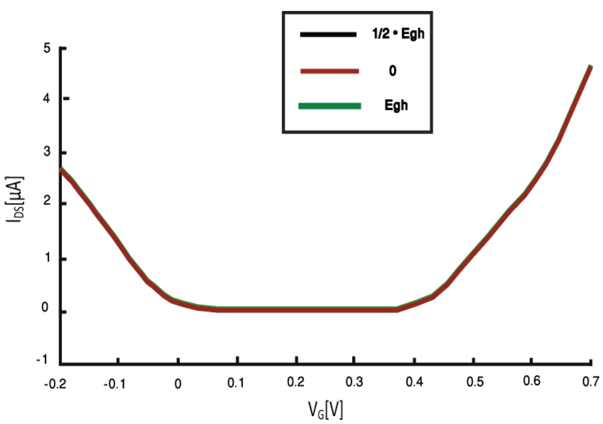

Fig. 12. Effect of different Schottky Barrier Height on I_{DS} vs. V_{GS}.

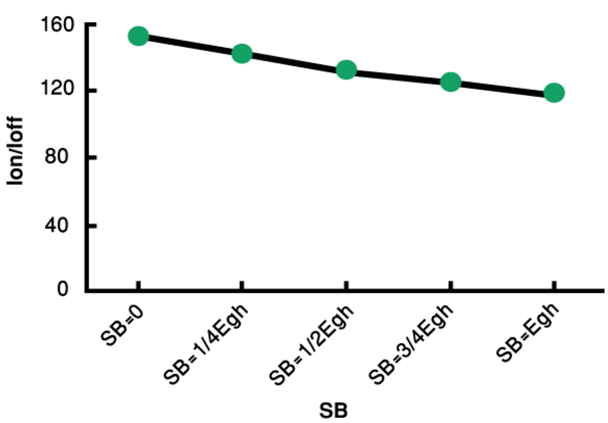

Fig. 13. Ion/Ioff ratio vs Schottky Barrier Height.

IV. Conclusion

In this work, the effect of gate insulator parameters on Ion/Ioff ratio for a SB_CNTFET has been studied for different parameters.

Current-voltage curve of theses transistors against gate length changes as well as changes to the on/off current in different gate length has been evaluated and it was clear at Gate length ($15nm \leq L_G \leq 40nm$) we have higher ratio. its clear that by reducing the thickness of the gate insulator, the ratio will increase (but at very low thickness the off current increased so the on/off current ratio decreased), Also it can be concluded according to the results that the use of materials with high dielectric constants, will lead to increase the on current and therefore on/off current ratio.

Its Empirically investigated, if the L_G/tox Ratio becomes lower than 18, so the on/off ratio will be reduced substantially.

At final, the effect of schottky barrier height changes studied and we found because of tunneling the electrons and holes, the on/off ratio will be decreased.

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Quantum Simulation of Double Halo Schottky Barrier CNTFET (DH_SB_CNTFET)

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Abstract_ In this paper, we performed a comprehensive scaling study of a schottky barrier carbon nanotube field-effect transistor (SB_CNTFET) with Double Halo doping using self-consistent and atomistic scale simulations. Our simulation results demonstrate that drain induced barrier lowering (DIBL) diminishes in the DH_SB_CNTFET due to the existence of a step in the potential of the CNT at the interface of doped and undoped regions in the channel. The effects of Double Halo structure on the static characteristics and switching speed performance for a carbon nanotube field effect transistor (CNTFET) have been theoretically investigated by a quantum kinetic model. This model is based on two-dimensional non-equilibrium Green's functions (NEGF) solved self-consistently with Poisson's equation. A comparison study of electrical characteristics in conventional Schottky Barrier CNTFET (SB_CNTFET) and Double Halo SB_CNTFET (DH_SB_CNTFET) structures has been performed. Simulations show that DH_SB_CNTFET significantly decreases leakage current and increases on current, on/off current ratio and Transconductance. The results indicate that cutoff frequency of the device, can be optimized by selecting the gate voltage.

Keywords_ SB_CNTFET, Carbon Nanotubes, Double Halo.

I. INTRODUCTION

The carbon nanotube field effect transistor is one among the most promising alternatives due to its superior electrical properties. Carbon nanotube field-effect transistors (CNTFETs) are a type of molecular transistor that has already demonstrated high on-currents[1].

As the thickness scales below 1.5 nm, leakage currents increase drastically, leading to high power consumption and reduced device reliability. The semiconductor industry is looking for different materials and devices to integrate with the current silicon based technology in a long term future.

Among the number of investigated solutions, carbon nano tubes (CNTs) are a promising material. Significant advances have been achieved in understanding device physics and improving device performance for carbon nanotube field effect transistors. One of the basic ideas is to replace the silicon MOSFETs with CNTFETs is to overcome all the limitations of silicon MOSFETs such as the exponential increase of leakage currents in scaled devices. These limits can be overcome to some extent and facilitate further scaling down of device dimensions by modifying the channel material in the traditional MOSFET structure with a single carbon nanotube[2].

In this paper we suggest double halo schottky barrier profile for the source and drain terminals. Our results demonstrate that the proposed DH_SB_CNTFET exhibits significantly reduced short-channel effects thus making it a more reliable device configuration than the SB_CNTFET for high performance CMOS circuit applications [3].

II. SB-CNTFET

To investigate the performance of aggressively scaled CNTFETs, we simulated a coaxially gated CNTFET with a 30 nm ballistic channel, as shown in Fig. 1 at room temperature (K) [4]. The nominal device has a 1 nm HfO_2 gate oxide (a high-gate insulator of this type has been experimentally demonstrated). The chiral vector of the nanotube is (8,0), which results in a bandgap of Eg=0.7eV. A power supply voltage of 0.4 V is assumed, according to the value specified for the 30 nm scale MOSFET, The device parameters here are the nominal ones. Carbon nanotube field-effect transistors were simulated by solving the Schrödinger equation using the nonequilibrium Green's function (NEGF) formalism self-consistently with the Poisson equation. Ballistic transport was assumed. An atomistic description of the nanotube using a tight binding Hamiltonian with an atomistic (Pz orbital) basis was used. The atomistic treatment was computationally expensive, but significant computational savings were achieved by the mode space approach. Because the carbon nanotube is coaxially gated, the eigenstates around the tube circumferential direction (modes) are plane waves with wave vectors satisfying the periodic boundary conditions. The two-dimensional (2-D) nanotube lattice of a(n,0) zigzag CNT was transformed to decoupled one-dimensional modes by doing a basis transform from the real space to the mode space in the circumferential direction (essentially Fourier transform). Under typical bias conditions, the few modes that are relevant to electronic transport are treated. The mode space approach reduces computation significantly yet retains atomistic resolution along the transport direction. For the i_{th} mode, the charge density is computed by integrating the local density-of-states (LDOS) over energy

$$Qi(t) = (-e) * \int_{-\infty}^{+\infty} dE . \operatorname{sgn}[E - E_N(Z)] * \left\{ D_{is}(E,Z) f(\operatorname{sgn}[E - E_{FS})) + D_{iD}(E,Z) f(\operatorname{sgn}[E - E_N(Z)](E - E_{FD})) \right\} \quad (1)$$

Where e is the electron charge, sgn(E) is the sign function, $E_{FS,D}$ is the source (drain) Fermi level, and $D_{iS,D(E,Z)}$ is the LDOS due to the source (drain) contact as computed by the NEGF method. Because the nanotube conduction and valence bands are symmetric, the charge neutrality level, $E_{N(Z)}$, lies at the middle of bandgap. The SBs at the metal/CNT interfaces were treated phenomenologically [4].

To mimic the continuous states injected from metal to the semiconducing nanotube modes, each semiconducting mode is coupled to the metallic mode of metallic zigzag CNTs at the M/CNT interface with the coupling described by two parameters. The first one is the band discontinuity at the interface, which is the SB height when there are no interface states. The second parameter is the tight-binding parameter between the semiconducting and the metallic mode, which determines to the density of metal–induced gap states (MIGS). This simple model describes the interface at a similar level as the M/CNT models in literature with the band discontinuity and density of interface states treated as input parameters.

A 2-D Poisson equation is solved to update the charge neutrality level in (1),

$$E_N(Z) = -e\phi(z, r = d/2) \tag{2}$$

where d is the nanotube diameter and ϕ (z) is the electrostatic potential

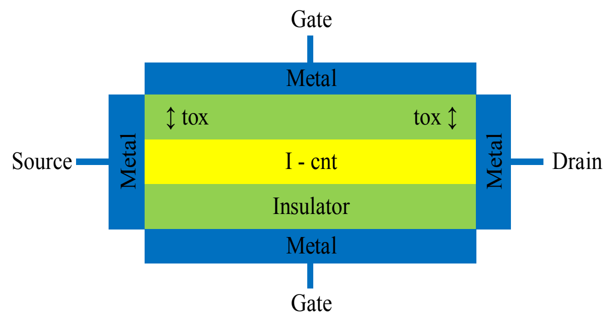
$$\nabla^2 \phi^2 (z, r) = -\frac{\rho}{\varepsilon} \tag{3}$$

The potentials at source-drain and gate electrodes are fixed as the boundary conditions, and the gate flat band voltage was as-sumed to be zero for simplicity. (In practice, it would depend on the gate workfunction.) In order to treat an arbitrary charge distribution on the nanotube channel, the Poisson equation is solved by the method of moments. The iteration between the atomistic quantum transport equation and the electrostatic equation continues until self-consistency is achieved, [a nonlinear form of (2) is used to improve the iteration convergence], then the source-drain ballistic current is computed by

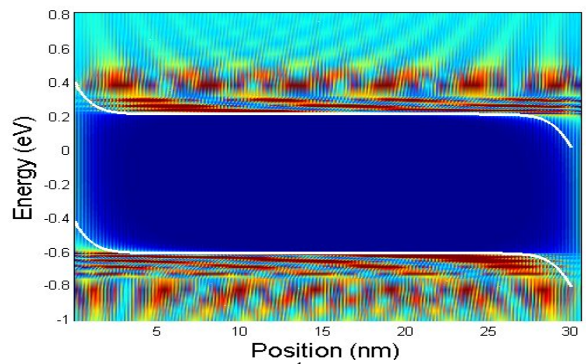
$$I = \frac{4e}{h}\int dE.[f(E-E_{FS}) - f(E-E_{FD})] \tag{4}$$

Where T(E) is the source-drain transmission calculated by the NEGF formalism. The gate leakage current is omitted in this study [4].

The transistor is coaxially-gated because this structure provides the best controlling state on channel by gate field, and consequently the minimum length of channel is needed[5]. The schematic of this device is represented in Fig. 1.



a

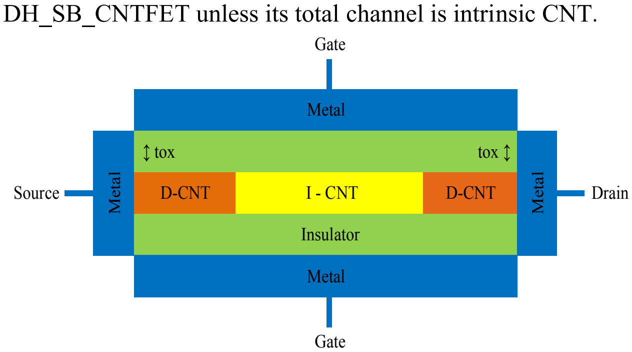


b

Fig. 1. a)Cross-sectional view of the SB_CNTFET, (8, 0) zigzag CNT, length across the device = 30 nm, gate insulator dielectric constant (κ) = 16, gate insulator thickness (tox) = 1 nm. b) Electron distribution function of SB_CNTFET.

III. DH_SB_CNTFET STRUCTURE

In the DH_SB_CNTFET, we consider a (8, 0) CNT which possesses a relatively large bandgap for reducing the band-to-band tunneling effect and SCEs. As shown in Fig. 2, we consider a CNT as a channel with a length of L=30nm and metal source/drain contacts. The CNT is embedded in a wrapped around HfO_2 layer with a thickness of 1 nm and dielectric constant of 16. The channel consists of p-doped CNT as a halo or pocket doped region with a length of 5nm. The length and concentration of the halo doped region on the source and drain sides of the DH_SB_CNTFET are kept at L_h=5 nm and N_h=1 nm^{-1}, respectively, unless otherwise stated. Other device parameters of the SB_CNTFET are equal to the DH_SB_CNTFET unless its total channel is intrinsic CNT.



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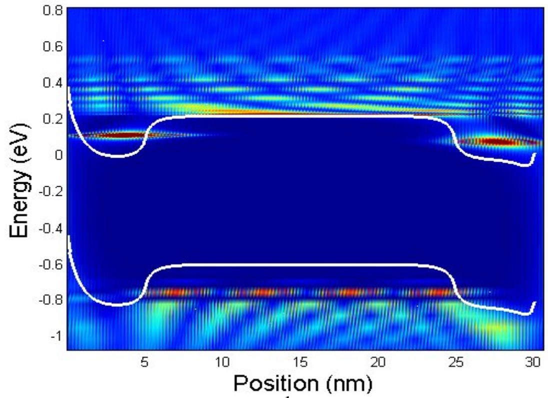


b

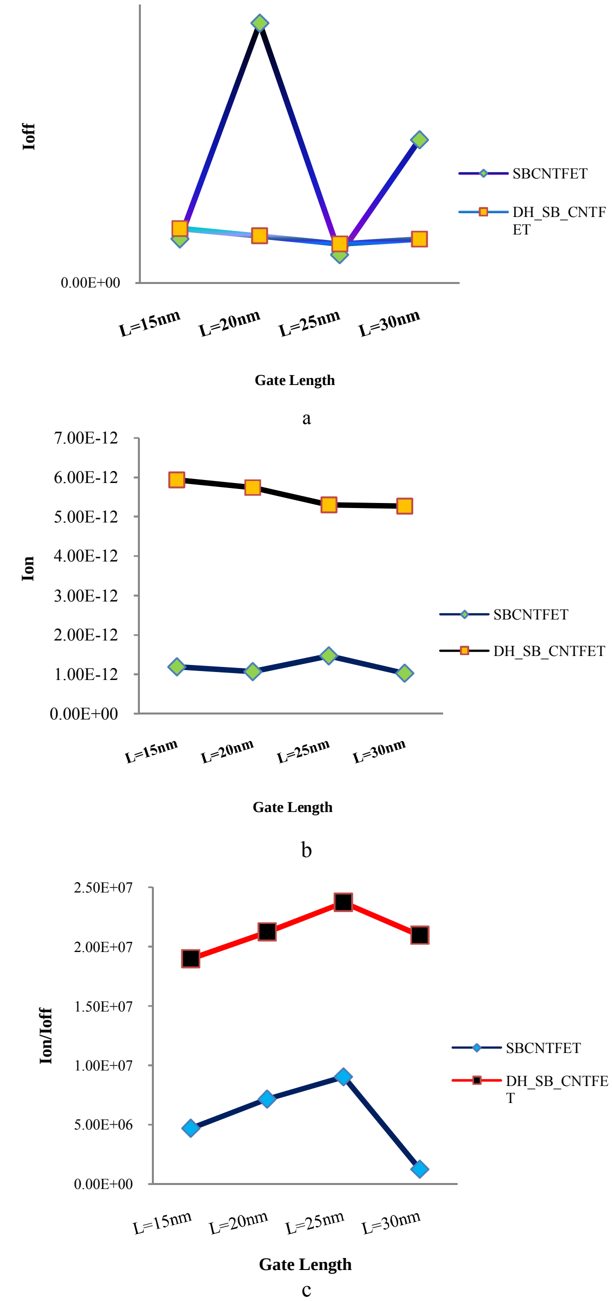
Fig2: Structure of DH_SB_CNTFET b) Electron distribution function of DH_SB_CNTFET.

The ambipolar behavior of two structures of SB_CNTFET is clearly observed from Fig. 4, in agreement with experimental and theoretical results. In n-type devices, applying a positive drain voltage decreases the energy barrier at the drain contact and consequently increases hole injection at this contact. In the on regime, the drain current increases with increase in the drain voltage. This ambipolar behavior limits the performance of the device. Due to the ambipolar behavior of SB_CNTFETs the off-current is intolerably high. This implies that not only the subthreshold slope and the on-current, but also the off-current increases. To avoid the ambipolar behavior of SB_CNTFETs and improve the performance of these devices, we propose double halo structure as shown in Fig. 2. If the drain voltage is applied to the Halo SB-CNTFET, at any drain voltage the energy barrier near the drain contact will be increased due to the p-doping of CNT near the drain. In consequence, the tunneling current of holes at the drain contact is suppressed and there is only some negligible thermionic emission current of holes. While electron injection at the source contact can be controlled through the p-doping region of CNT near the source, the p-doping region of CNT near the drain suppresses parasitic hole current at the drain contact.

In this simulation, the z and r direction are discretized with a grid spacing of a=0.25 nm and b=0.1 nm, respectively. The simulation is carried out at room temperature (T=300° K).

IV. RESULTS AND DISCUSSION

To further investigate the scaling potential of proposed new structure, the comparisons have been made among the two structures of SB_CNTFET at different channel lengths. The variations of off-state current, on-state current, and on/off current ratio versus channel length are plotted in Fig. 3. The on current and off current are defined as the channel current when Vg=Vds=0.4v and Vg=0v, Vds=0.4v, respectively. In Fig. 3(a), it is observed that for double halo structure, longer channel will lead to lower off-state currents. This is due to the fact that as channel length increases, the gate controls on the electrostatic of channel region enhanceand consequently the leakage currents diminish dramatically. It can also be that Halo SB_CNTFET structures can reduce off-state current which is mainly caused by the Halo structure. Fig. 3(b) shows the on-state current, it is noted that the on-state current (Ion) of two structures remains approximately constant, which indicates that the ballistic on-state current is nearly independent of the channel length with the gate length range from 15 to 30nm. So the on/off current ratio improves with an increase of the length (see Fig. 3(c)).



c

Fig.3 Variation of (a) Ioff and (b) Ion and (c) Ion/Ioff of four structures of SB_CNTFETs with channel leng that Vgs=Vds=0.4 V.

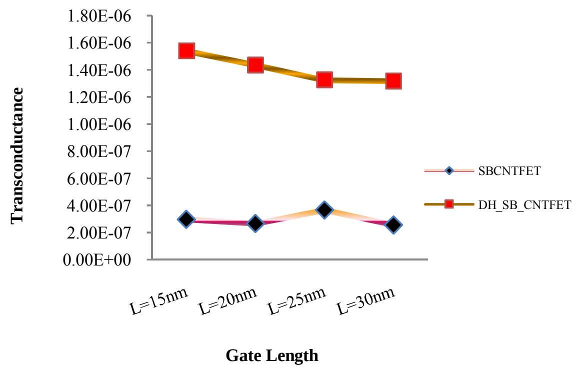


Fig. 5. Variation of Transconductance with channel length.

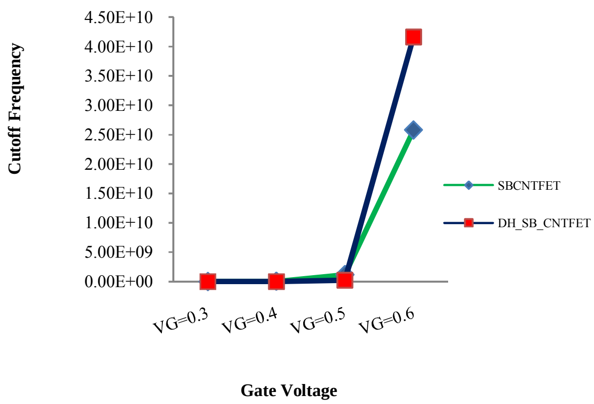


Fig. 5. Variation of Cutoff Frequency with Gate voltage.

The variations of transconductance (gm) and cutoff frequency (Ft) are shown in Fig. 4 and 5. As shown in Fig. 4, longer channel length leads to lower transconductance for Double Halo SB_CNTFET. This is primarily due to an increase in channel length that results in a larger effective channel length, which reduces SCE and DIBL. In Fig. 5, we found that the intrinsic cut-off frequency keeps increasing approximately as the gate voltage is 0.5v to 0.6v range.

CONCLUSIONS

In this paper, the behavior of nanoscale MOS like CNTFET with Schottky contact is theoretically studied with a quantum kinetic model. This quantum kinetic model is based on two-dimensional NEGF solved self-consistently with Poisson's equations. The electrical characteristics of a novel nano scale Schottky Barrier CNTFETs, with combination of Double Halo structure, have been investigated. Results reveal that compared with the conventional structures, double Halo Schottky Barrier CNTFETs significantly decreases leakage current and increases on/off current ratio, indicating that the proposed structure has better gate controllability than conventional Schottky Barrier CNTFETs. The influence of channel length on current characteristics has been studied. The simulations show that longer channel can decrease off-state currents, while the ballistic on-state current (Ion) of two structures remains approximately constant. the cutoff frequency of the device, can be optimized by reasonably selecting the Gate voltage. A new result concerning optimum range of doping level and length reported in this paper requires experimental verification through device fabrication.

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Performance Optimization of Conventional Schottky Barrier CNTFETs Based on Stair-Case Halo Doping Strategy

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Abstract**-- For the first time, a schottky barrier carbon nanotube Field-Effect Transistors (SB_CNTFETs) is proposed and simulated using quantum simulation then Comparisons are made for electrical characteristics among two SB_CNTFETs structures, which are conventional Schottky Barrier CNTFETs and Stair Case Halo Doping structure SB_CNTFETs. The results show that the Stair Case Halo Doping structure decreases significantly the leakage current, Increases On current, so increases On/Off current ratio as well as cutoff frequency. Finally, the subthreshold swing of the two structure of SB_CNTFETs have been discussed. It is noticeable Stair Case Halo Doping structure has the small subthreshold swing, so the Stair Case Halo Doping structure has a better ability of suppressing the DIBL.**

Keywords: Schottky Barrier CNTFET, Halo Doping, Quantum Simulation.

I. INTRODUCTION

Today, two major types of CNTFETs have been introduced: Schottky barrier CNTFETs (SB_CNTFETs) and MOSFET like CNTFETs (MOSCNTs). SB_CNTFETs are made by contacting an intrinsic CNT to the metal electrodes. In SB_CNTFETs the dominant mechanism of delivering current is tunneling through Schottky barriers at the source and drain junctions. Due to the contribution of both electrons and holes in conduction, SB_CNTFETs exhibit ambipolar characteristics and suffer from small on and high off currents. To overcome these shortcomings, the second type of CNTFETs known as MOSFET like CNTFETs (MOSCNTs) with doped terminals has been developed. The carbon nanotube can form Ohmic contacts with metal electrodes if it is doped with the appropriate dopant usually potassium[1]. MOSCNTs have higher on and lower off currents than SB_CNTFETs and behave like normal MOSFETs because in these transistors the Schottky barriers' width at the source and drain contacts and thus the ambipolar conduction have been suppressed. The dominant mechanism of delivering current in such transistors is the thermionic emission which is controlled by modulating the barrier in the intrinsic region of the channel by using appropriate gate voltages. However in this case, tunneling of the electrons from valence band to the conduction band and vice versa constitutes a leakage current that increases the total current in high reverse gate voltages and prevents MOSCNTs from being unipolar perfectly. Because of the smaller bandgap of large diameter CNTs, the band to band tunneling is more severe when the CNT diameter is larger. There have been attempts to develop MOSCNTs with reduced ambipolarity by changing the doping level or using a non-symmetric oxide thickness. In this paper we suggest schottky barrier profile for the source and drain terminals. Our results demonstrate that the proposed HD_SB_CNTFET exhibits significantly reduced short-channel effects thus making it a more reliable device configuration than the SB_CNTFET for high performance CMOS circuit applications [1].

II. SCHOTTKY BARRIER CNTFET

To investigate the performance of aggressively scaled CNTFETs, we simulated a coaxially gated CNTFET with a 30 nm ballistic channel, as shown in Fig. 1 at room temperature (K) [2]. The nominal device has a 1 nm HfO_2 gate oxide (a high-gate insulator of this type has been experimentally demonstrated). The chiral vector of the nanotube is (8,0), which results in a bandgap of Eg=0.7eV. A power supply voltage of 0.4 V is assumed, according to the value specified for the 30 nm scale MOSFET, The device parameters here are the nominal ones. Carbon nanotube field-effect transistors were simulated by solving the Schrödinger equation using the nonequilibrium Green's function (NEGF) formalism self-consistently with the Poisson equation. Ballistic transport was assumed. An atomistic description of the nanotube using a tight binding Hamiltonian with an atomistic (Pz orbital) basis was used. The atomistic treatment was computationally expensive, but significant computational savings were achieved by the mode space approach. Because the carbon nanotube is coaxially gated, the eigenstates around the tube circumferential direction (modes) are plane waves with wave vectors satisfying the periodic boundary conditions. The two-dimensional (2-D) nanotube lattice of a(n,0) zigzag CNT was transformed to decoupled one-dimensional modes by doing a basis transform from the real space to the mode space in the circumferential direction (essentially Fourier transform). Under typical bias conditions, the few modes that are relevant to electronic transport are treated. The mode space approach reduces computation significantly yet retains atomistic resolution along the transport direction. For the i_{th} mode, the charge density is computed by integrating the local density-of-states (LDOS) over energy

$$Q(t)=(-e)*\int_{-\infty}^{+\infty} dE\,\mathrm{sgn}[E-E_N(Z)]*$$
$$\left\{D_{is}(E,Z)f(\mathrm{sgn}[E-E_{FS}))+D_{iD}(E,Z)f(\mathrm{sgn}[E-E_N(Z)](E-E_{FD}))\right\} \quad (1)$$

Where e is the electron charge, sgn(E) is the sign function, $E_{FS,D}$ is the source (drain) Fermi level, and $D_{iS,D(E,Z)}$ is the LDOS due to the source (drain) contact as computed by the NEGF method. Because the nanotube conduction and valence bands are symmetric, the charge neutrality level, $E_{N(Z)}$, lies at the middle of bandgap. The SBs at the metal/CNT interfaces were treated phenomenologically [2].

To mimic the continuous states injected from metal to the semiconducing nanotube modes, each semiconducting mode is coupled to the metallic mode of metallic zigzag CNTs at the M/CNT interface with the coupling described by two parameters. The first one is the band discontinuity at the interface, which is the SB height when there are no interface states. The second parameter is the tight-binding parameter between the semiconducting and the metallic mode, which determines to the density of metal–induced gap states (MIGS). This simple model describes the interface at a similar level as the M/CNT models in literature with the band discontinuity and density of interface states treated as input parameters.

A 2-D Poisson equation is solved to update the charge neutrality level in (1),

$$E_N(Z)=-e\phi(z,r=d/2) \quad (2)$$

where d is the nanotube diameter and ϕ (z) is the electrostatic potential

$$\nabla^2\phi^2(z,r)=-\frac{\rho}{\varepsilon} \quad (3)$$

The potentials at source-drain and gate electrodes are fixed as the boundary conditions, and the gate flat band voltage was assumed to be zero for simplicity. (In practice, it would depend on the gate workfunction.) In order to treat an arbitrary charge distribution on the nanotube channel, the Poisson equation is solved by the method of moments. The iteration between the atomistic quantum transport equation and the electrostatic equation continues until self-consistency is achieved, [a nonlinear form of (2) is used to improve the iteration convergence], then the source-drain ballistic current is computed by

$$I=\frac{4e}{h}\int dE.[f(E-E_{FS})-f(E-E_{FD})] \quad (4)$$

Where T(E) is the source-drain transmission calculated by the NEGF formalism. The gate leakage current is omitted in this study [2].

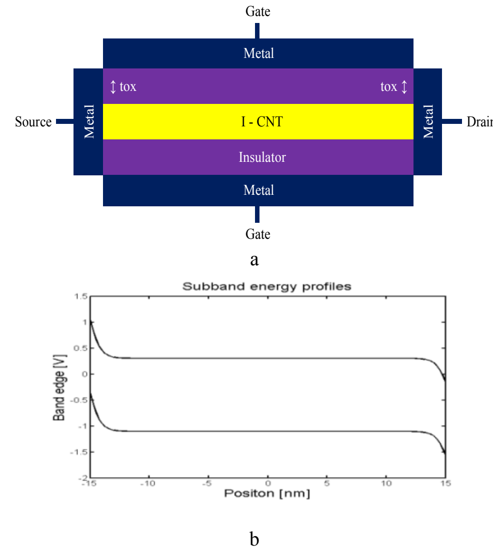


Fig. 1. Structure of SB_CNTFET b) Energy-position of SB_CNTFET

III. STAIR-CASE HALO DOPING STRATEGY

In the HD_SB_CNTFET, we consider a (8, 0) CNT which possesses a relatively large bandgap for reducing the band-to-band tunneling effect and SCEs. As shown in Fig. 2, we consider a CNT as a channel with a length of L=30nm and metal source/drain contacts. The CNT is embedded in a wrapped around Hfo_2 layer with a thickness of 1 nm and dielectric constant of 16. The length and concentration of the halo doped region on the source side of the HD_SB_CNTFET are kept at L_{D1}=2.5 nm and N_{D1}=1.5 nm^{-1} and at the Drain side L_{D1}=L_{D2}=2.5nm (5nm total), N_{D1}=1.5nm^{-1} and N_{D2}=0.15nm^{-1}. Other device parameters of the SB_CNTFET are equal to the HD_SB_CNTFET unless its total channel is intrinsic CNT.

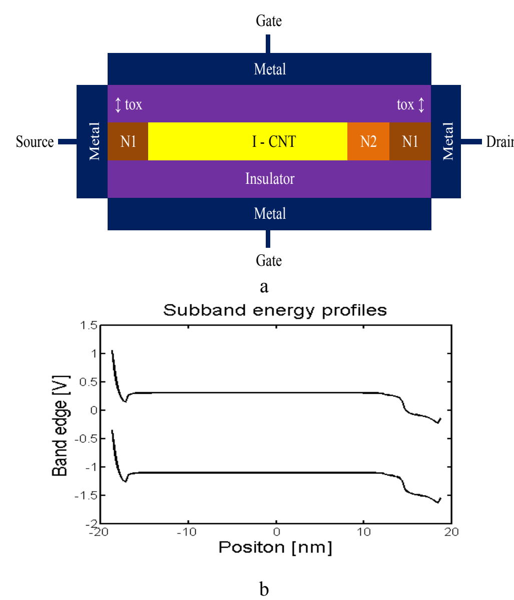
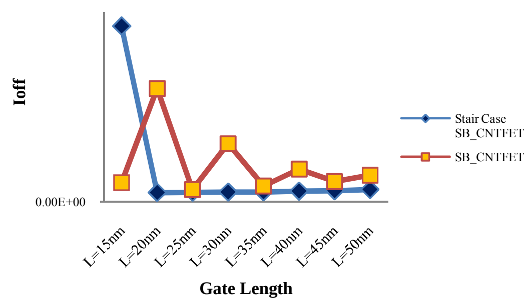


Fig. 2. Structure of SH_SB_CNTFET b) Energy-position of SH_SB_CNTFET

IV. RESULTS AND DISCUSSION

Using the described semi-classical model, the current of the stair case halo doping SB-CNTFET has been calculated and the dependence of its magnitude on the bias voltages has been investigated. The source contact is assumed to be ground. In Fig. 3(a), it is observed that for stair case halo doping structure, longer channel will lead to lower off-state currents. This is due to the fact that as channel length increases, the gate controls on the electrostatic of channel region enhanceand consequently the leakage currents diminish dramatically. It can also be that Halo SB_CNTFET structures can reduce off-state current which is mainly caused by the Halo structure [3]. Fig. 3(b) shows the on-state current, it is noted that the on-state current (Ion) of two structures remains approximately constant, which indicates that the ballistic on-state current is nearly independent of the channel length with the gate length range from 20 to 50nm. So the on/off current ratio improves with an increase of the length (see Fig. 3(c)).



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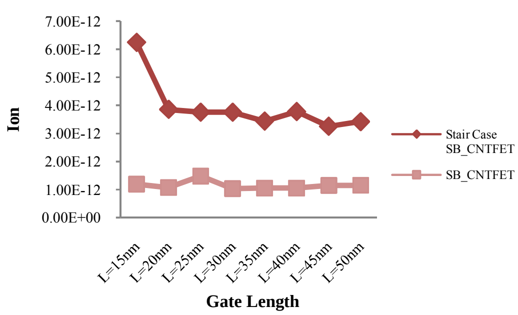

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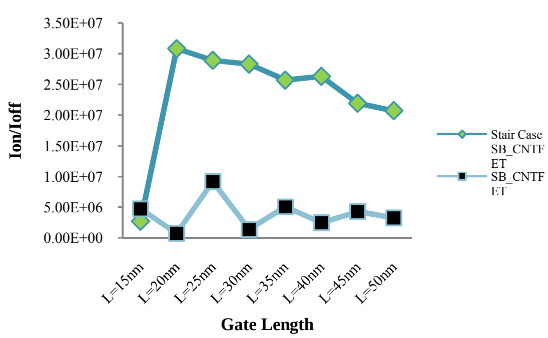

c

Fig. 3. Variation of (a) Ioff and (b) Ion and (c) Ion/Ioff of two structures of SB_CNTFETs with Vgs=Vds=0.4 V.

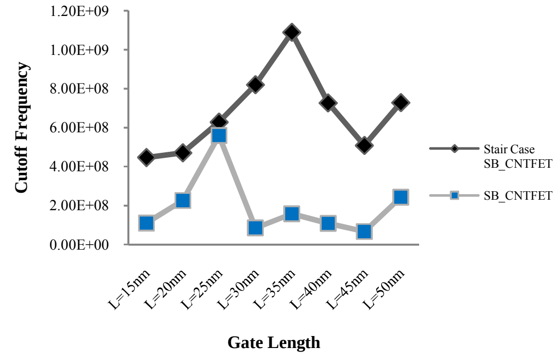

Fig. 4. Variation of Cutoff Frequency of two structures of SB_CNTFETs with Vgs=Vds=0.4 V.

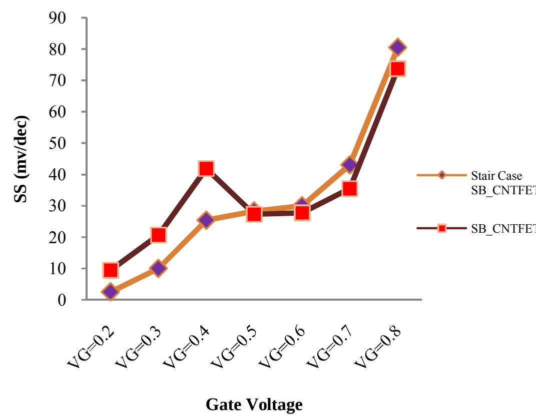

Fig. 5. Variation of SS (mv/dec) of two structures of SB_CNTFETs with 30nm channel length.

The variations of Cutoff frequency and SS(mv/dec) with channel length and voltage are shown in Fig. 4, 5. As shown in Fig. 4, at the 35nm channel length we can obtain highest cutoff frequency for Halo structure SB_CNTFET and Subthreshold swing of Stair Case Halo and C-CNTFET at 30nm channel length are compared in Fig. 5. It is evident from the figure that Halo Doping SB_CNTFET shows reduced subthreshold swing in comparison with SB_CNTFET at gate voltage lower than 0.5v. This is attributed to superior control of the gate voltage of Halo Doping SB_CNTFET over the channel.

V. CONCLUSION

The new structure of coaxial asymmetrical contacted CNTFET with Schottky types of contacts at the source and drain was introduced. Because of a lower on current in comparison with conventional SB_CNTFETs, the device has the potential of being used in low bias ultra-high speed integrated circuits. The simulation has shown that because of reduction of band-to-band tunneling of electrons between the conduction and valence in the SC_HD_SB_CNTFET, this structure significantly reduces leakage current when compared to that of a SB_CNTFET. The SC_HD_SB_CNTFET also exhibits higher On current and finally higher Ion/Ioff ratio, also higher cutoff frequency and lower SS(mv/dec) compared

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to the SB_CNTFETs, which make them good candidates for future high-performance CMOS circuit applications.

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A Novel 0.5V Bulk Driven Pseudo-Differential OTA

Antaryami Panigrahi , Abhipsa Parhi

***Abstract*—**A novel low voltage bulk driven pseudo-differential OTA is presented here. It operates at a supply of 0.5V. Operations of the OTA are analyzed theoretically and confirmed with the simulation. The simulated results show open loop gain to be 24dB and UGB of 330 kHz and Phase Margin of 80°. The input referred noise is 60uV/$\sqrt{Hz}$, Slew Rate 12V/uSec for load of 1pF and 10kΩ. Simulated transient response shows, the OTA achieving full swing of 100mV_{p-p}. The circuit is designed using 250nm twin-well CMOS and simulated using T-Spice and BSIM 3v3 model. The power dissipation of the proposed OTA is 6.4µWatts.

***Keywords*—**Bulk driven Analog circuit; Low-voltage Circuit design ;OTA; Pseudo-differential OTA .

I. Introduction

THE scaling of digital CMOS technology makes the analog circuit design quite challenging, sharing the Si-space with digital circuits on the same substrate poses even more challenge. And the demand for low power portable and battery operated systems has veered analog circuit design towards smart use of transistors in weak inversion or in boundary of weak and moderate inversion losing significant band width and matching properties [1], [2], [3]. This technique has been used for many applications [4], [5], [6], [7], [8], where low power operation is prime importance. Sometimes weak inversion mode has been successfully exploited for emulating trans-linear property of BJT devices in digital CMOS technology for performing arithmetical operations. Another smart approach has been using the bulk terminal to forward bias the source-substrate junction (assuming no parasitic-bipolar–action) and losing the DC gain, increasing the input referred noise since g_{mb} is 4 to 5 times smaller than g_m. But this approach allows the devices to operate at much lower $|V_{DS,sat}|$, so allowing the circuit to use the least supply voltage. There are many works reported using this approach for various applications [9], [10], [11], [12], [13]. At the circuit level, reducing the no of stacked transistors allows the circuits to operate at much lower supply voltage. Designing the OTA at such lower voltage dropping the tail current source opens the gate for pseudo-differential technique [13], which helps in getting full swing at such low supply voltage. Many adaption of pseudo-differential OTA has been reported in [10], [11], [12]. Getting higher gain has been a daunting task with bulk driven pseudo-differential OTA because of low bulk-transconductance. Recent trends in analog circuit design in Lower nanometer technologies pushes the circuit designers towards the use of Bulk terminal to dynamically vary the threshold. A number of works [10], [11], [12], [13], [14] is reported in literature. In this work a new technique of Pseudo-differential OTA is presented driving the bulk terminals with the cross-coupled transistors. Full operation of the circuit is explained in section II. Bulk driven circuit used here is inherently susceptible to threshold voltage variations, so the mismatch analysis is explained and expression for input referred offset voltage is derived in Section III in addition to the noise contributed by the circuit. The circuit is simulated and results are shown and discussed in Section IV.

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II. The Proposed Pseudo-differential OTA

The input transconductance (g_{mb}) is obtained using partial positive feedback with the help of bulk driven pMOS transistors MP1& MP4. Gate terminals of both the input transistors MP1, MP4 are tied to the ground to make sure that transistors operate in strong inversion. MN1 & MN. The partial positive feedback [9] is used for introducing negative g_{mb} which is formed by the cross coupled pair of MP2 & MP3. Another cross coupled pair formed by connecting the gate-to-drain of MN2 & MN3 introduces another negative transconductance g_m. This further improves the gain by 2-3 dB. MP7& MP5 with zero gate bias are connected which improves the output resistance of the Pseudo-Differential OTA. The gates of the NMOS transistors are biased such that all the transistors operate in strong inversion and in the saturation mode. The NMOS devices are given a forward substrate bias of 200mV to decrease the threshold voltage by 150mV, such that the devices operate in strong inversion even at a small gate bias of 100mV. Differential gain of the OTA can be calculated with the help of the small signal equivalent shown in figure 2. The expression for the DC gain is;

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$$A_{diff} = \frac{g_{mb1}}{g_{ds1}+g_{ds2}+g_{ds3}+g_{ds4}+g_{ds5}-g_{mb3}-g_{m4}} \qquad (1)$$

Where g_{mb3} and g_{m5} are the transconductances due to the cross coupled transistors and $g_{ds,i}$ are the output conductances (i=1, 2...5) to get a positive DC gain, the denominator has been made quite small and positive (order of 11×10^{-6}) with proper biasing. The amount of negative conductance added to the denominator terms can be controlled with the help of substrate bias voltages to vary the respective V_{TH} values of the cross-coupled pair, in other way to vary the gate conductance and bulk-conductance. Since the dependence of g_m and g_{mb} on the substrate bias are related as;

$$g_m = \mu_n . C_{ox} . \frac{W}{L}\left[V_{GS} - V_{T0} + \gamma\left(\sqrt{2\phi_F + |V_{SB}|} - \sqrt{2\phi_F}\right)\right];$$

where V_{T0}, γ are the terms as expressed in [15]. And g_{mb} is written as in [15];

$g_{mb} = g_m . \frac{\gamma}{\sqrt{2\phi_F + |V_{SB}|}}$; assuming the devices in Saturation.

The common mode voltage is 0.25V. The input bulk-transconductance is of the order of 100uAmp/Volts. The differential gain obtained from the proposed OTA is 24 dB. The expression for common-mode gain can be written as;

$$A_{cm} = \frac{g_{mb1}}{g_{ds1}+g_{ds2}+g_{ds3}+g_{ds4}+g_{ds5}+g_{m4}} \qquad (2)$$

The g_{m4} term is larger than g_{mb1} making the common mode gain quite small i.e. -70dB. Unlike that of [10], where a local common mode feedback with help of resistor is used to sense the common mode level and to bring down the common mode gain, we get lot more common gain without using any extra circuitry for common mode feedback. In the process area can be saved and thermal noise contribution due to the resistors can be avoided.

III. Mismatch and Noise Analysis of the OTA

A. Analysis of Mismatch

For two identically designed devices of a differential pair biased with identical V_{GS}, there can be two main sources of mismatch in the drain currents i.e. V_{TH} and β . The mismatch in drain currents can cause the DC offset [5]. For bulk driven transistors in a pseudo-differential pair, the extra mismatch due to the mismatch in the substrate bias voltages and also due to difference in bulk-effect coefficients results in an extra degradation of the matching of the transistors. With the help of Taylor's Series Expansion around a substrate bias of V_{SB} can be derived. The following well known expression [15] for V_{TH};

$$V_{TH} = V_{T0} + \gamma\left(\sqrt{2\phi_F + |V_{SB}|} - \sqrt{2\phi_F}\right) \qquad (3)$$

Shows the dependence of V_{TH} and substrate bias V_{SB}. Two transistors biased with V_{SB2} and V_{SB1}, (Assuming Gate terminal

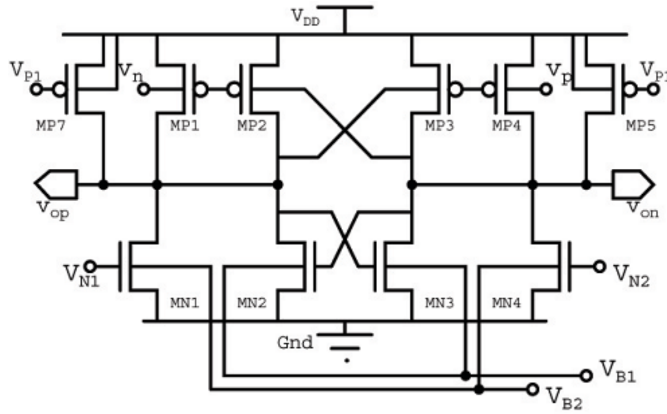

Figure 1 Proposed Pseudo-differential OTA

is at same bias for both the devices, V_{GB} remaining same) the deviation in the threshold voltage can be derived by expanding the Eq. (4) using Taylor's Series around a DC operating point V_{SB};

$$\Delta V_{TH} = \Delta V_{T0} + \Delta\gamma\sqrt{2\phi_F} + \Delta\gamma\sqrt{2\phi_F + |V_{SB}|} + \frac{1}{\sqrt{2\phi_F + |V_{SB}|}}(\gamma_1 . V_{SB1} + \gamma_2 . V_{SB2} - \Delta\gamma . V_{SB}) + \cdots \qquad (4)$$

The above expression shows the extra mismatch terms due to substrate bias and body coefficients. The matched pairs of the proposed OTA from Fig. 1 are: M_{P1}, M_{P4}; M_{N1}, M_{N4}; M_{P2}, M_{P3}; M_{N2}, M_{N3}; M_{P5}, M_{P7} ,which can represented as : $M_{1A,B}$, $M_{2A,B}$, $M_{3A,B}$, $M_{4A,B}$, $M_{5A,B}$ respectively to simplify our derivations. The input referred offset voltage due to mismatch in the current for each pair of matched pair of transistors can be calculated as in [15].The variance of the input referred offset due to $M_{1A,B}$ can be written as;

$$\sigma^2_{v_{in1}} = \left[\frac{\sigma(\Delta\beta 1)}{\beta 1}\right]^2 . \frac{I^2_{D1}}{g^2_{mb1}} + \sigma^2(\Delta V_T),$$

$$\sigma^2_{v_{in3}} = \left[\frac{\sigma(\Delta\beta 3)}{\beta 3}\right]^2 . \frac{I^2_{D3}}{g^2_{mb1}} + \frac{g^2_{mb3}}{g^2_{mb1}} . \sigma^2(\Delta V_T),$$

$$\sigma^2_{v_{in4}} = \left[\frac{\sigma(\Delta\beta 4)}{\beta 4}\right]^2 . \frac{I^2_{D4}}{g^2_{mb1}} + \frac{g^2_{mb4}}{g^2_{mb1}} . \sigma^2(\Delta V_T), \text{ and}$$

$$\sigma^2_{v_{in5}} = \left[\frac{\sigma(\Delta\beta 5)}{\beta 5}\right]^2 . \frac{I^2_{D5}}{g^2_{mb1}} + \frac{g^2_{mb5}}{g^2_{mb1}} . \sigma^2(\Delta V_T) .$$

So variance of total offset voltage can be expressed as;

$$\sigma^2_{v_{ios}} = \sigma^2_{v_{in1}} + \sigma^2_{v_{in2}} + \sigma^2_{v_{in3}} + \sigma^2_{v_{in4}} + \sigma^2_{v_{in5}} \qquad (5)$$

Where $\beta_i = \mu_n . C_{ox} . \left(\frac{W}{L}\right)_i$ and $\frac{\sigma(\Delta\beta)}{\beta} = \frac{A^2_{\beta}}{W.L}$; $\sigma^2(\Delta V_T) = \frac{A^2_{VT}}{W.L}$.

A_{VT} and A_{β} are the process constants as given in [5]. It can be inferred from eqn. (6), input referred offset voltage can be decreased by decreasing the input bulk-transconductance of the OTA i.e. g_{mb1} due to the $M_{1A,B}$.

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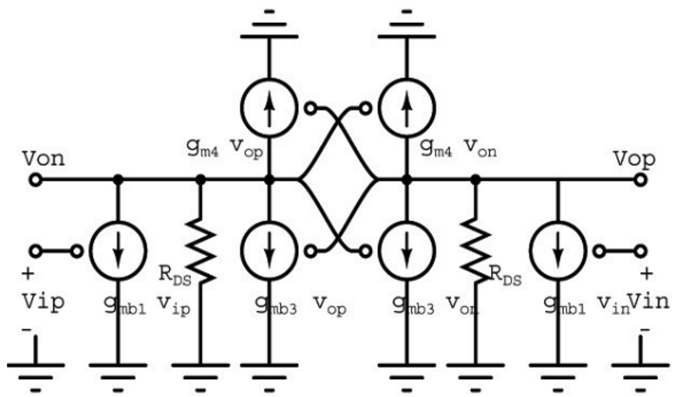

Figure 2 Small signal Model of the proposed OTA

The ratio of g_m/g_{mb} being less than unity causes severe problems in input referred offset at such low supply voltages [13].

B. Analysis of Noise

Assuming the noise sources in each half of the OTA are uncorrelated their effects on the output can considered individually. Two main sources of noise that can affect the performance of the OTA are: flicker Noise and thermal noise. The expression for Flicker Noise can be written as;

$$\overline{v_{n(1/f)}^2} \approx \frac{K_f}{g_{mb1}^2 . C_{ox} . f}\left[\frac{g_{m1}^2}{(WL)_1} + \frac{g_{m2}^2}{(WL)_2} + \frac{g_{m3}^2}{(WL)_3} + \frac{g_{m4}^2}{(WL)_4} + \frac{g_{m5}^2}{(WL)_5}\right] \quad (6)$$

Ignoring the thermal noise component due to the Gate resistance and Bulk resistance, the approximated thermal noise expression can be written as;

$$\overline{v_{n(Th)}^2} \approx \frac{4.K.T.\gamma}{3.g_{mb1}^2}\left[g_{m1} + g_{m2} + g_{m3} + g_{m4} + g_{m5}\right] \quad (7)$$

The above expression shows that the bulk input devices are more susceptible to the flicker noise component owing to the lower value of g_{mb} than gate input devices and larger value of g_m/g_{mb} ratio.

IV. Results and Discussions

To verify the circuit performance, 250nm twin well CMOS technology is used to simulate the proposed circuit, using BSIM 3v3 model in TSPICE. The CMOS process has V_{THN} and V_{THP} = 0.45 Volt. To operate the circuit the supply voltage used is of 0.5 V. In this work, the bias currents of all transistors are chosen to optimize both gain and power dissipation. An AC signal of magnitude 1V, 10 kHz is applied to the circuit with load capacitance of 10pF and resistance of 10kΩ. The simulated gain and phase response of the circuit is shown in Fig. 3 and 4 respectively. It can be seen that the DC gain is approximately 24dB, UGB is around 331 kHz. The phase margin is around 80 degree from Fig. 4. The transient response of the circuit is obtained by simulating the

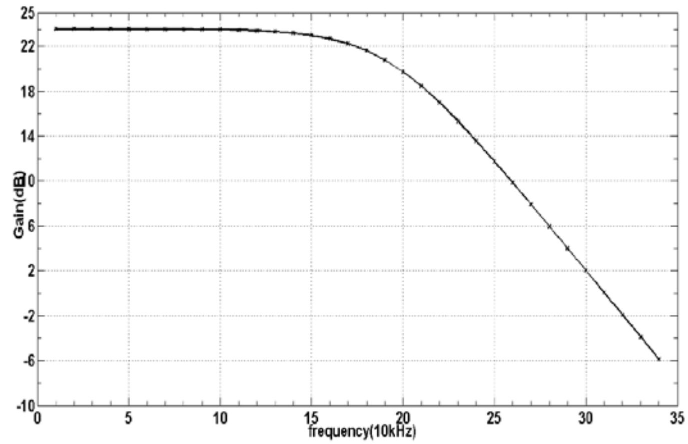

Figure 3 Gain Response of the OTA

circuit with a common mode 0.25V and sinusoidal signal of 10 mVp-p,10 kHz at its input. As it can be seen from Fig. 5, that output common mode voltage is maintained around 0.25V

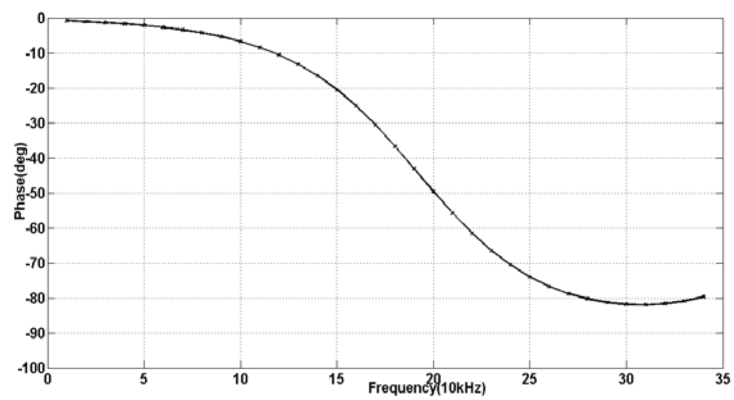

Figure 4 Phase response

(the dotted line in Fig. 5) and output swings between 140 mV to 360 mV. Single ended output is shown in Fig. 5 to show the DC common mode voltage at the outputs.

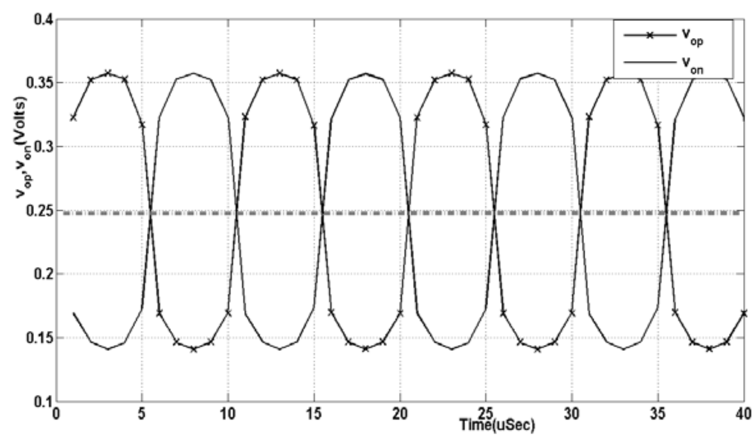

Figure 5 Transient output (single ended)

To simulate for the slew rate of the OTA, a pulse of time period 100 nSec (having 5nSec rise and fall time) is applied to the OTA, the transient response is shown in Fig. 6. The slew

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rate from the response can be found to be 4.64V/µSec with same load conditions (10pF, 10kΩ). Total power dissipation by the circuit 6.4µW. The summaries of simulated results are

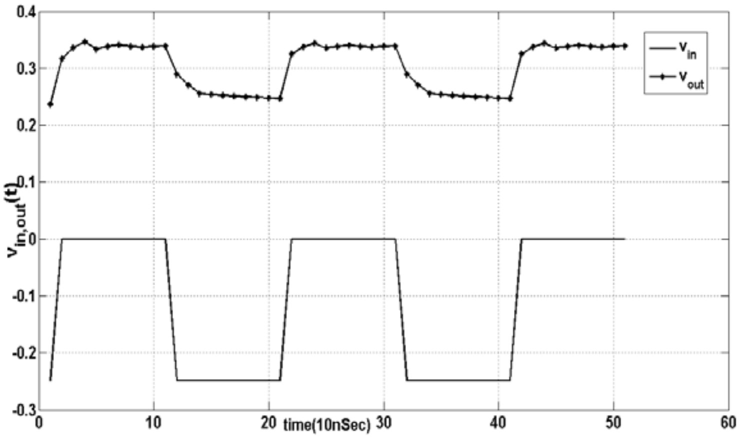

Figure 6 Transient response for a pulse input (Single ended)

shown in the Table-I. Input referred noise for this OTA is on higher side, as the flicker noise dominates at lower frequencies and the ratio of g_m / g_{mb} is also lower.

Table 1 Performance Summary of the OTA

Parameters	***Simulated values***
Power (uW)	6.4
DC gain(dB)	23.5
GBW(kHz)	320
Phase Margin(deg)	80
Input Referred Noise(µV/$\sqrt{Hz}$) at UGB	64.59
CMRR(dB) at UGB	-94 dB
Slew Rate(V/µSec)	4.64

V. Conclusion

A new technique of implementing bulk driven pseudo-differential OTA at 0.5V is presented. The proposed technique is analyzed thoroughly mathematically and the simulated results confirm the operation of the OTA having a DC gain of 24dB from a single stage OTA. Common mode gain is quite low around -70dB. Thermal noise contributed by this OTA is on higher side, as the problem of flicker noise still remains with bulk driven circuits.

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A Novel Design of Low-power SRAM cell

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Abstract—SRAM cell is one of the most important part of FPGAs and Caches in digital design domain. This paper presents a new 8T SRAM cell with better performance (power consumption and delay time) than regular 6T and 8T SRAM cells. HSPICE simulations show that this new 8T SRAM cell has at least 43.7% improvement at power consumption in comparison with 6T SRAM cell based on 7nm technology model.

Keywords—SRAM cell; power consumption; delay time; standby power; nanotechnology

I. INTRODUCTION

A digital system such as a computer is required memory to store data. Static Random Access Memories (SRAM) is usually made based on CMOS technology. In recent years the demand for low power devices has been increases tremendously. Also at the same time problems arising from continuous technology scaling have recently made power reduction an important design issue for the digital circuits and applications. SRAM based cache memories are best suited for system on chip applications due to its high speed and low power consumption.

One of the most effective approaches to meet this objective is to design SRAM cells whose operation is low power. However, with the aggressive scaling in technology, substantial problems have been encountered when the conventional six transistors (6T) SRAM cell configuration is utilized. In conventional SRAM cell because one of two bit-lines must be discharged to low (regardless of written value) the power consumption in both writing "0" and "1" are generally same [1]. Also during read operation, one of the two bit-lines must be discharged [3]. Therefore always there are transitions on bit lines in both writing "0" and reading "0". These cause high dynamic power consumption during read/write operation in conventional 6T SRAM cell. This cell shows poor stability at very small feature sizes and read static noise margins are small at 7nm. Therefore, an extensive literature can be found on designing SRAM cells for low power operation in the deep sub-micron/nano ranges [2] [4]. The common approach to meet the objective of low power design is to add more transistors to the original 6T cell. An 8T cell can be found in [2]; this cell employs two more transistors to access the read bit-line.

This paper proposed a new design for SRAM cell encountered in deep sub-micron CMOS ranges (7nm). This cell is that its design requires 8 transistors (8T). The process of the new 8T cell is compared with conventional 6T & 8T [2] cells. It is shown that this cell is better than 6T & 8T cells in terms of power consumption, stability, and access time. Simulation results using HSPICE confirm that the proposed new 8T cell is suited for implementation at 7nm CMOS technology, PTM models are used for HSPICE simulations.

II. SRAM CELLS

A. Conventional 6T SRAM cell

Current and read static noise margin (SNM) are two important parameters of SRAM cell. The conventional 6T SRAM cell has been found to be rather unstable at deep submicron/nano scale technology. The read SNM of cell shows the stability of cell during read operation and SRAM cell current determine the delay time of SRAM cell [5]. Fig. 1 shows the SRAM cell current in the conventional SRAM cell. Both Read SNM and SRAM cell current values are highly dependent on the driving capability of the access NMOS transistor. Read SNM decreases with increases in driving capability, while SRAM cell current increases [5]. That is, the dependence of the two is in an inverse correlation.

For solving the problem of inverse correlation between SRAM cell current and read SNM, a dual-port SRAM cell is composed of eight transistors, proposed in this cell data retention element and data output elements are separated each-others there for there will be no correlation between Read SNM and SRAM cell current.

B. Existing 8T SRAM cell

To solve the decreased read SNM problem, the read and write processes are separated by adding read access structures to the conventional 6T cell. The read current does not affect the cell value, then the read stability of the 8T cell [2] is increased. Fig. 2 shows the scheme of an 8T SRAM cell. Write access to the cell occurs through the write access transistors (i.e. N1-N4, P1, P2) is identical to a conventional 6T SRAM cell and from the write bit-lines, BL and BLB. Read access to the cell is through the read access transistor N7, N8. This transistors are employed in to reduce the leakage current. Read operation controlled by the read word-line, RWL. Read bit-line, RBL is precharged prior to the read access. The word-line for read is also different from the write word-line.

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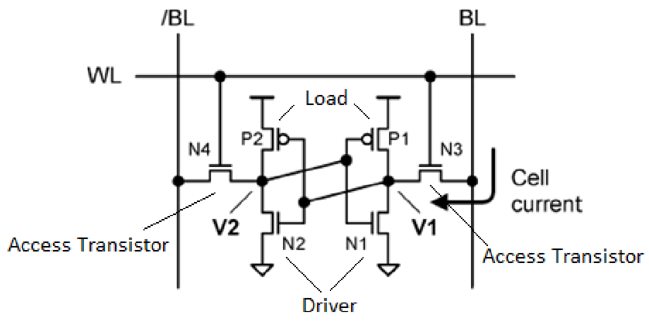

Fig. 1. Conventional SRAM cell

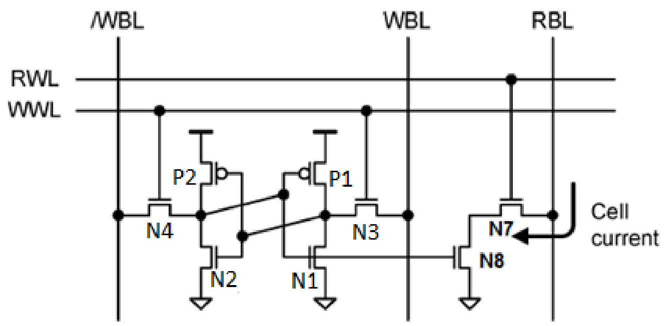

Fig. 2. Existing 8T SRAM cell

By doing this the worse-case stability position encountered previously in a 6T SRAM cell, is avoided and high read stability is retained prescribed; please do not alter them. You may note peculiarities. For example, the head margin in this template measures proportionately more than is customary. This measurement and others are deliberate, using specifications that anticipate your paper as one part of the entire proceedings, and not as an independent document.

C. New 8T SRAM cell

Fig. 3 shows a nodified new 8T SRAM cell. Data protection NMOS transistor N5 for loop-cutting has been added between Node V2 and transistor N2. In our proposed new 8T-cell, V_{th} in the NMOS N2 transistor are reduced, making it possible to achieve both low-V_{dd} and high-speed operations. During write mode of cell While the SRAM cell is being accessed, /WWL is in the inactivated state, “0”, and N5 is OFF. Since N5 prevents the voltage at node V2 from decreasing, the data bit is not reversed even if node V1 voltage greatly exceeds. standby mode of cell read and write operation don’t perform on cell but signal /WWL is “1”, and transistor N5 is ON. The use of two CMOS inverters conclusions in high cell stability [Fig. 6, Fig. 7]. Figure 8 shows that the proposed new 8T cell has a higher
read SNM, comparing to the 8T SRAM cell.

One of the major advantages of this design is that it is necessary to prepare a precharge circuit as required in existing 8T SRAM cell and it is not necessary a sense amplifier circuit as required in 6T SRAM cell. Only when the RBL is changed, a charge/discharge power on the RBL is consumed.

III. Read and Wright Operation

During write operation read-line (RWL) and /WWL maintained at GND. A write operation the memory cell will go through the following steps.

1) Bit-line driving: For a write, data drove on bit-line (WBL), and then word-line (WWL) asserted to VDD.

2) Cell flipping: this step includes two states as follows:

a) Data is zero: in this state, V2 node pulled down to GND by NMOS access transistor (N4), and therefore the Load transistor (P1) will be ON, and V1 node will be pulled up to VDD. Fig. 4 shows scheme of write "0" in the circuit.

b) Data is one: in this state, V2 node pulled up to VDD by NMOS access transistor (N4), and therefore the drive transistor (N1) will be ON, and V1 node will be pulled down to GND.

3) Precharge mode: The read bit-line, RBL , is precharged prior to the read access.

A read operation the memory cell is composed of two series transistors (N3 and N6) will go through the following steps. The word-line for read is also different from the write word-line. To start the read operation:

1) RWL activation: For a read, read bit-line precharged to vdd, and then floated. and read-word-line asserted to VDD during read operation.

2) Write-word-line inactivation: in this step write-word-line asserted to GND and two states can be considered:

a) Voltage of V1 node is high: when voltage of V1 node is high, RBL pulled down to GND through the transistor stack formed by N3 and N6. Fig. 5 shows scheme of read "0" in the circuit.

b) Voltage of V1 node is low: when voltage of V1 node is low, RBL remained to VDD becouse thetransistor N3 will be off.

3) Standby mode: At the end of read operation, cell will go to standby mode (when read and write operation don’t perform on cell) and read&write-word-line asserted to GND, respectively.

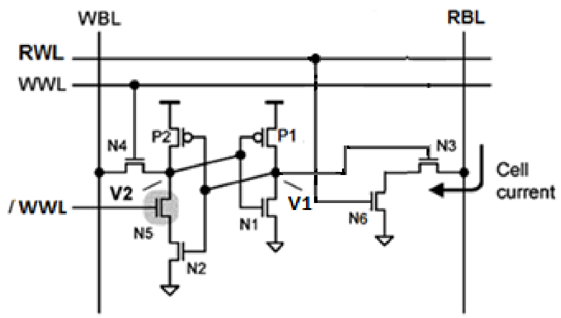

Fig. 3. New 8T SRAM cell

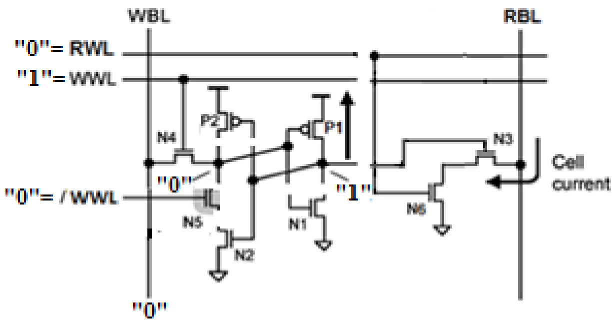

Fig. 4. Write "0" operation

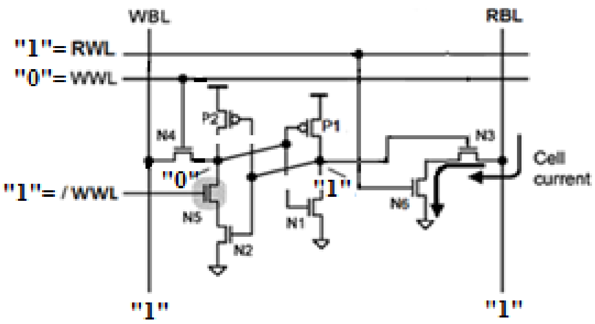

Fig. 5. Read "0" operation

IV. Power Dissipation

Write power consumption of single ended structure is less because the bit line capacitance is reduced as compared to 6T double bit line switching.

$$Ps = \alpha ClVdd^2F_{cl} \quad (1)$$

Where Ps is switching power dissipation, α is activity factor, Cl is load capacitance and Vdd is power supply, F_{cl} is input clock frequency [6].

As shown in Figure 9, the write power is significantly reduced with the proposed new 8T SRAM cell as compared to the conventional 6T SRAM cell. This reduction is due to the application of a single bit line for writing into the 8T SRAM cell in a memory column. For the 6T SRAM cell both bit lines in each memory column are periodically precharged to Vdd. When write operatione is constructed, one of the precharged bit lines is selectively discharged to Vss to do a write operation. Therefore, one of the bit lines needs to be fully charged and discharged during each write cycle, regardless of whether a 0 or a 1 is transferred to the cell. In case of writing a "1" to a memory column with the new 8T SRAM cell, the write bit line (WBL) does not need to be discharged. Then power consumption is significantly reduced. During read operation, the read power consumption is significantly reduced with the proposed new 8T SRAM cell as compared to the conventional 6T SRAM cell because the storage nodes (V2, V1) are completely isolated from the bit lines during a read operation.

V. Simulation Results

In this section comparison between conventional 6TSRAM, new8T SRAM cell and 8T SRAM cell has been carried out on the basis read delay, average standby power and read & hold SNM (Table 1).

TABLE I. Comparison of average power dissipation during Standby operation , access time during read operation and read & hold SNM with the different combination of single VT and Low Vdd at 0.7v and 0.6v

SRAM Cell	Supply Voltage(v)	Read SNM(v)	Hold SNM(v)	Av Standby Power(nw)	Read Access Time(ns)
6T	0.7	0.0711	0.125	297.33	1.4
	0.6	0.0915	0.050	230.97	1.35
Existing 8T	0.7	0.196	0.125	241.67	2.7
	0.6	0.119	0.0502	195.71	2.45
New 8T	0.7	0.203	0.217	229.83	2.75
	0.6	0.138	0.153	183.24	2.65

As you can see in Figure 8 by increasing the amount of voltage SNM increased and by reducing the amount of voltage SNM is reduced.

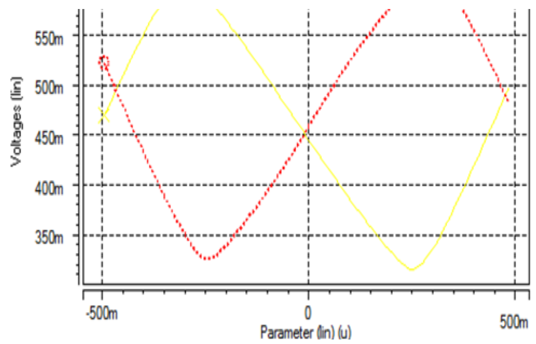

Fig. 6. Rotated (45°) Read SNM butterfly plot of a new 8T SRAM cell

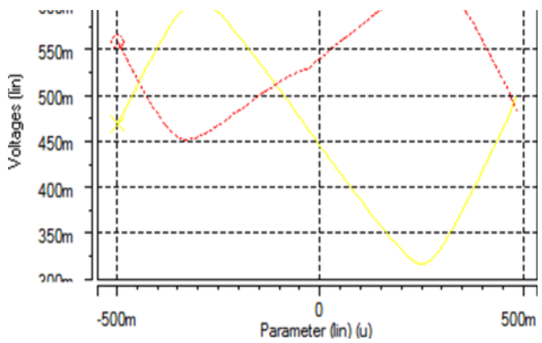

Fig. 7. Rotated (45°) Hold SNM butterfly plot of a new 8T SRAM cell

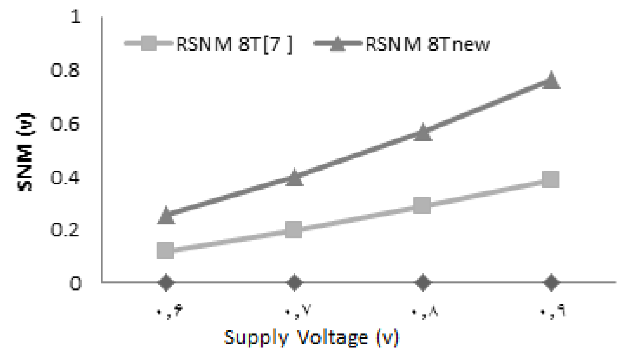

Fig. 8. Chart increase SNM by increasing the source voltage

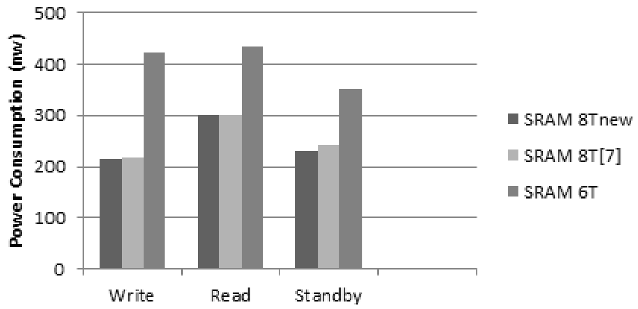

Fig. 9. Read,write and standby power consumption at 0.7V

VI. CONCLUSION

The new 8T SRAM has been compared with respect to conventional 6T SRAM. Read delay of 8T SRAM cell is 20%, 0.5% better than 6T SRAM cell and 8T SRAM cell, because of the lower resistance of the read access delay path. Write delay of 8T SRAM is higher than conventional 6T SRAM and existing 8T SRAM cells due to utilization of only a single bit line for writing into the cells with the proposed technique.

New 8T SRAM when stored "0" and "1" respectively, has 49.16%, 54.02% less write power consumption as compared to 6T SRAM cell, and has 1.14%, 16.37% less than 8T SRAM cell [2]. This reduction in the write power is due to the utilization of a single bit line for writing into the new 8T and 8T SRAM [2] cells in a memory.

Read power consumption of new 8T SRAM when stored "0" and "1" respectively, is 30.53%, 43.72% better than 6T SRAM cell, and is 0.1%, 3.15% better than 8T SRAM cell due to advantage of low voltage of bit line during read operation.

In standby mode, power consumption of new 8T SRAM when stored "0" and "1" respectively, is 34.40%, 38.26% less than 6T SRAM cell, and is 4.89%, 5.53% less than 8T SRAM cell [2]. All the above simulations are done by 600mv as supply voltage and is shown a significant power reduction than regular cells.

The HSNM & RSNM & WSNM of new 8T respectively, is 42.39%, 3.44%, 12.14% high than 8T SRAM cell [2].

It is shown that this cell is better than 6T & 8T [2] cells in terms of power consumption, stability, and access time. Simulation results using HSPICE confirm that the proposed new 8T cell is suited for implementation at 7nm CMOS technology, PTM models are used for HSPICE simulations.

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A Novel Method for Transistor Sizing in Digital Circuits by Artificial Intelligence

Eghbal Rahimi, Seyyed Reza Talebiyan

***Abstract*—**in this paper a new optimization method is proposed for transistor sizing of VLSI digital circuits based on artificial intelligence. The optimized dimensions are especially conducted for minimizing power dissipation (dynamic and static power) and delay.
In order to verify the efficiency of the proposed method, transistor's dimensions of four well-known full-adder circuits in different frequencies and voltage levels are optimized and their results are compared to the previously reported results. Simulation results of HSpice provided in TSMC 0.18μm technology, show considerable improvement of power delay product (PDP) reduction. The results promise a strong impact since full-adders are the basic block in the most VLSI circuits.

***Keywords*—**Transistor Sizing, Artificial Intelligence, Digital Circuits, Electrical Simulation

I. Introduction

In transistor sizing of digital circuits, designers always face a trade-off between delay and power dissipation. Transistor sizing is not a difficult task in small circuits in contrast to the complexes. In complex circuits, it takes too much time for a designer to achieve the desired results, considering the fact that the results even may not be optimized at all. Recently automatic designing of digital circuits based on CAD (Computer Aid Design) tools has grabbed considerable attention which has resulted in a vast improvement in evolutionary algorithms [1], [2].
Full-adders are known as a basic blocks in computer arithmetic [3]. These blocks are non-separable parts of any microcontroller, DSP, FPGA and other processors. These basic blocks are responsible for most of calculations in the processors. So Full-adders transistors size optimization will result in PDP reduction .Reaching a fine method for optimization could be so effective especially when the number of full-adders increases in complex circuits. Fishburn et al.[4] and Sapatnekar [5]et al. used convex program to reach the desired delay. The program is known as a classic non-smart method with a high possibility of getting stuck in local minimum. Chang et al.[6] optimization method has the previous problems and also is more time-consuming. Most importantly, steps employed for (transistor sizing) optimization is a non-integer multiply of λ which could cause a drawback in fabrication process.
In this paper an automatic design toolbox for size optimization applied in four well-known full-adder circuits. Thus a powerful genetic algorithm is employed in order to get optimized transistors' dimensions. The reminder of the paper is organized as follows. In section II, automatic sizing tool is introduced. In section three, transistor's dimension and simulation results are presented. In the fourth part the goal function is evaluated and the final conclusion is presented

II. Automatic Design Tools

The optimization tool of transistor's dimensions is based on a mutual connection between Matlab and Hspice. So a genetic algorithm [7] is employed in order to get the optimized dimensions of transistors. The proposed method is applied in four well-known full-adder, Hybrid CMOS [8], New 14T [9] and improvement of PDP is subjected. The schematic of these circuits are shown in Fig. 1.

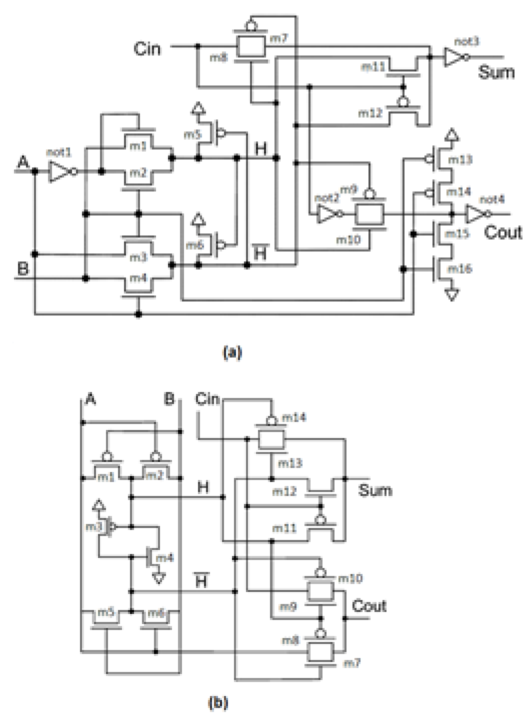

Fig. 1 Full adder cells of different logic styles (a) Hybrid CMOS (b) New 14T

Before running the automatic design tool, an empty SP file should be created. Circuit topology, its technology and type of

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the demand simulation, form the content of the mentioned file. The optimization methodology could be described in four steps. 1) Creating a set of responses for independent variables. 2) Entering the responses into the SP file as an input for Hspice and running simulation program. 3) Extracting the account of the goal functions from the output file 4) Evaluating the goal functions. In continue these steps will be explained briefly.

1-cerating set of responses for independent variables: the Independent variables are transistors' dimensions which are the output of the automatic design tool. For the first run, the independent variables are filled with random data, after that each time the independent variables will be updated through applying genetic algorithm over the previous data. The produced data are the results of two operators, crossover (choosing parents and combine them for reproduction) and mutation (choosing some part of population to produce mutant).

Crossover and mutation input populations can be selected in three ways, randomly, among the best responses or combination of both. In the proposed algorithm the population is selected completely random, but in crossover operator sufficiency of responses are also considered in possibility of selection (roulette wheel selection). The chromosome production base on transistor dimensions is shown in Fig. 2.

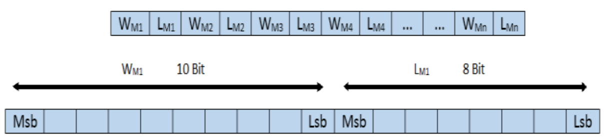

Fig. 2. Genetic algorithm chromosome representation

2- Entering the responses into the SP file as an input for Hspice and running simulation program: as mentioned, before running the simulator a SP file as net list should be created which contains transistors' dimensions in parametric. In continue the first responses are loaded into the SP file. Each time that responses are loaded, MATLAB send a run instruction to the HSPICE which updates the output results.

3- Extracting the account of the goal functions from the output file: goal functions in digital circuits can be defined in many parameters as for example power consumption, delay or PDP. For extracting each one, some extra code should be considered in both SP file and MATLAB. In the proposed algorithm minimizing PDP was subjected in order to produce data extracting codes.

In proceeding of extracting program, another important parameter known as penalty has been added [10]. In order to verify the optimized responses, the output results should match with truth table of a full-adder. Considering the mismatch between responses and truth table, parameter of fine is assigned to responses. When the procedure of optimizing is finished the value of fine parameter should be equal to zero and PDP should be at its minimum.

4- Evaluating the goal functions: after each run, goal functions corresponding to their responses are saved and classified based on their values. In crossover and mutation operators these classifications will be needed in order to choose parents populations.

For each iteration, at first, the classification is applied. Then to run crossover operator, parents are chosen based on roulette wheel selection and start to reproduce [11]. The reproduction is also followed by mutation operator. The produced children (which are the responses of independent variables) are entered into the SP file one by one. Finally, the simulation is run and goal functions are extracted. This cycle is continued until the fine parameter becomes zero and PDP becomes as small as possible. Fig 3 shows mentioned four steps as a filo chart.

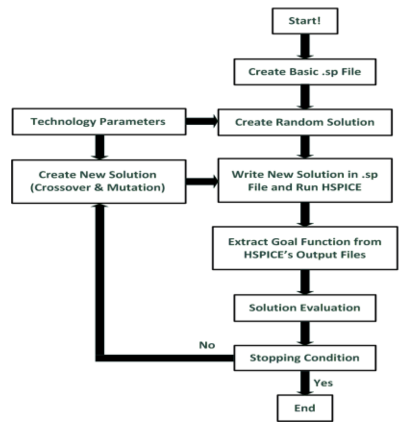

Fig 3.Designed flow for the transistor sizing using genetic algorithms

Two full-adder circuits, Hybrid CMOS and New 14T, in two power supply levels, 1.2V and 1.8V, and at three frequencies of 100MHz, 200MHz and 500MHz were subjected to optimization. The choice of power supply levels and frequencies are based on vast applications of these numbers. The results approve the efficiency of automatic design tool. The circuits were simulated using HSPICE on TSMC 0.18µm technology level 49. The calculated power consumption is the average power which consist of static, dynamic and short circuit power consumption. Circuit in Fig. 4 [8] was used to get as close as possible results to real circuits. The numbers showed at the top and bottom of NOTs are dimensions according to 2λ.

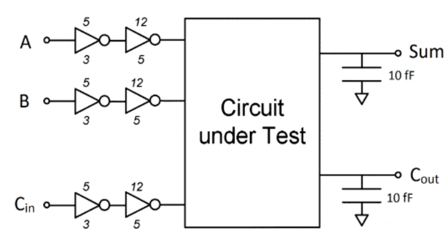

Fig.4 test bench

III. TRANSISTOR'S DIMENSION AND RESULTS

In this section the optimized dimensions of transistors of two full-adders are compared and discussed. The optimized transistors' dimensions of Hybrid CMOS and New 14 are shown in Tables 1 to 2, respectively. In the Tables, length and width of each transistor is integer multiply of λ.

Table 1. Hybrid CMOS

Dimension	Vdd=1.2 V			Vdd=1.8 V		
	F=100	F=200	F=500	F=100	F=200	F=500
M1	11/2	5/2	20/2	6/2	8/2	6/2
M2	3/2	4/2	3/2	3/2	5/3	3/2
M3	3/2	4/2	5/2	3/3	9/2	3/2
M4	11/2	10/2	9/2	19/2	20/3	10/2
M5	4/2	3/2	5/2	3/2	5/2	3/2
M6	10/2	7/2	8/2	11/2	11/2	8/2
M7	3/2	3/2	3/3	3/2	3/2	3/3
M8	3/2	3/2	3/3	3/2	3/2	4/2
M9	7/2	3/2	5/2	4/2	4/2	3/2
M10	3/2	3/2	3/2	3/2	4/2	3/3
M11	7/2	8/2	7/2	8/2	5/2	11/2
M12	3/2	3/2	4/2	3/3	3/2	3/3
M13	6/2	4/2	3/2	9/2	3/2	8/2
M14	5/3	3/2	3/2	3/2	3/2	3/2
M15	3/2	4/2	3/2	3/2	3/2	3/2
M16	4/3	3/3	3/2	6/3	4/3	3/2
Not1-p	11/2	5/2	7/2	7/2	6/2	7/2
Not1-n	3/2	3/2	4/2	4/2	5/2	3/2
Not2-p	11/2	5/2	7/2	7/2	6/2	7/2
Not2-n	3/2	3/2	4/2	4/2	5/2	3/2
Not3-p	11/2	5/2	7/2	7/2	6/2	7/2
Not3-n	3/2	3/2	4/2	4/2	5/2	3/2
Not4-p	11/2	5/2	7/2	7/2	6/2	7/2
Not4-n	3/2	3/2	4/2	4/2	5/2	3/2

Table 2. New 14

Dimension	Vdd=1.2 V		Vdd=1.8 V		
	F=100	F=200	F=100	F=200	F=500
M1	31/2	31/2	21/2	18/2	20/2
M2	31/2	31/2	19/2	19/2	18/2
M3	27/2	31/2	20/2	12/2	10/2
M4	3/2	3/2	3/2	3/2	3/2
M5	3/2	4/2	21/2	7/2	7/2
M6	4/2	3/2	8/2	4/2	3/2
M7	3/2	3/2	3/2	7/2	4/2
M8	3/2	3/2	3/3	3/2	3/2
M9	3/3	4/3	3/2	3/3	3/3
M10	3/2	4/3	4/2	3/2	3/2
M11	4/2	3/2	13/2	9/2	8/2
M12	3/3	3/2	3/3	3/3	3/3
M13	3/2	3/3	3/2	3/2	4/2
M14	5/2	3/2	3/2	12/2	16/2

Simulation results of the proposed designs and the original full-adder circuits in references are shown and compared in Table.

Table 3. Hybrid Cmos

Frequency (MHz)	Voltage (V)	Our PDP	PDP	Improvement (%)
100	1.2	6.5309e-15	9.3901e-15	30.4
100	1.8	8.3488e-15	1.2598e-14	33.7
200	1.2	1.1272e-14	1.9068e-14	40.8
200	1.8	1.6089e-14	2.3677e-14	32.0
500	1.2	3.0253e-14	4.4984e-14	32.7
500	1.8	3.5920e-14	5.7156e-14	37.1

Table 4. New 14

Frequency (MHz)	Voltage (V)	Our PDP	PDP	Improvement (%)
100	1.2	1.6856e-14	3.7609e-14	55.1
100	1.8	1.0164e-14	1.4602e-14	30.3
200	1.2	3.1559e-14	3.5607e-13	91.1
200	1.8	1.5943e-14	2.8115e-14	43.2
500	1.2	---	---	---
500	1.8	3.9429e-14	6.7594e-14	41.6

IV. Conclusion

In this paper, transistor sizing of a digital circuit (adder) is done by using meta-heuristic algorithms. This kind of sizing results in a great improvement in PDP. With respect to the simulation results by usage of this method in these two adder circuits an improvement of 30% to 90% in PDP is achievable. The optimum size of the transistors is the final result of this kind of meta-heuristic optimization. The size of transistors are presented as an integer multiply of λ.

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A 10-bits three channels phase shifter integrated circuit for Active Electronic Scanned Array applications

G. Coviello, G. Piccinni, G. Avitabile, N. Margiotta

Abstract**—**The paper describes a 10-bits three channels phase shifter in 0.35 µm SiGe BiCMOS technology. The chip was designed for control an Active Electronically Phase Array (AESA). It is composed by a digital Phase Control Block (PCB) which generates square waves with a minimum phase shift of 0.3515° and an output frequency of 1.953MHz; the system clock is 2GHz. Besides the PLLs and the VCOs are external components in order to validate the frequency-independence of the architecture proposed. As expected from the simulations, the maximum phase error is less than 0.1° and the rms phase error is less than 0.06°. The complete systems at 2.45GHz with almost the same maximum phase error and rms confirm the validity of the architecture.

Keywords**—**Phase Shifter, Phased Arrays, integrated circuit, PLL.

I. INTRODUCTION

PHASE shifters are very critical blocks in Electronically Scanned Arrays (ESAs). Indeed they allow varying the phase of each element of array. In this case any mechanical movements are not necessary, reducing costs and sizes of system. The other main advantages of these structures are high directivity, interference rejection, fast scanning response and signal to noise ratio improvement.

In literature there are many architectures of phase shifter related to the ESA scheme. It is possible to divide these architectures into three groups. The first one includes the distributed-type phase shifters (DTPSs) [1]. The phase shifters which use a vector sum of two or more orthogonal-phased signals belong to the second group [1]-[3]. Depending on the signal direction this group can be subdivided in forward-type and reflective-type phase shifter (FTPSs, RTPSs). The last group is formed by the phase shifter that uses an all-pass network [4]. The phase shifter can be of digital (discrete phase shift) or analog (continuous phase shift) type.

In this paper an integrated circuit implementation of an evolution of the architecture proposed in [7]-[9] is presented.

Section II describers the phase shifter basic operation and the system architecture. The simulation results are shown in the Section III while in the Section IV the prototype description and experimental results are discussed; finally a conclusion is given in Section V.

II. PHASE SHIFTER OPERATION

In Fig. 1 it is shown the architecture proposed; it is based on the scheme presented in [9] but in this implementation the accumulator has been replaced with a simple counter. This leads to an improvement in terms of power consumption, complexity and area occupied.

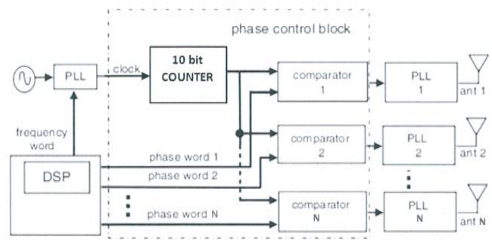


Fig. 1 Phase Shifter Architecture

The system is composed by a 10-bits counter which drives the N comparator, N PLLs driven by the wanted mutually shifted signals generated by the comparators and a DSP or microcontroller which imposes the phase control word to each digital comparator. The basic idea is to use the PCB to generate the phased square waves at low frequency, and the PLLs to upconverting the signal without worsening the phase shift imposed by the PCB. The output frequency of the PCB is

$$f_{OUT} = \frac{f_{CLK}}{2^{10}} = \frac{2GHz}{2^{10}} = 1.953MHz \quad (1)$$

where f_{CLK} is the system clock frequency. Moreover the minimum phase step is:

$$\Delta\emptyset = \frac{360°}{2^{10}} = 0.3515625° \quad (2)$$

As for the topology presented in [7], also in this case there is the possibility of using an M divider in the feedback path of the PLL instead of a mixer (Offset-PLL) without worsening the phase resolution. It is enough to choose an odd value and to use a Look-up table to rearrange the output phase shifts.

An aspect very relevant for this architecture is that it is a frequency independent. In fact as said the PLLs have to upconverter the signal preserving the phase shift imposed by the PCB. So changing the PLLs and the VCOs we change the output frequency but not the phase resolution. For this reasons the PLLs and the VCOs are left off-chip, in order to test this topology at different frequency.

The Integrated Circuit was realized in 0.35 µm SiGe BiCMOS process provides by AustriaMicroSystem. This process is cheaper than conventional CMOS processes, but does not exhibit excellent performance for frequencies above approximately 500 MHz. However the design of the elementary cells (inverter , NAND / NOR gates, etc.) in emitter coupled logic, has allowed to realize the system with a maximum clock frequency of 2 GHz.

The design of chip includes one 10-bits counter and three 10-bits comparators, so the system is able to provide the control signals for a phased array composed by three elements.

The core of chip occupies an area of 3.781 x 2.481 mm^2; the final layout is depicted in Fig. 2 and a picture of the naked chip in Fig. 3.

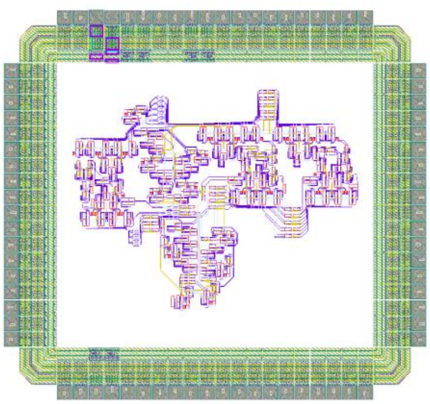


Fig. 2: Phase Shifter – Final Layout

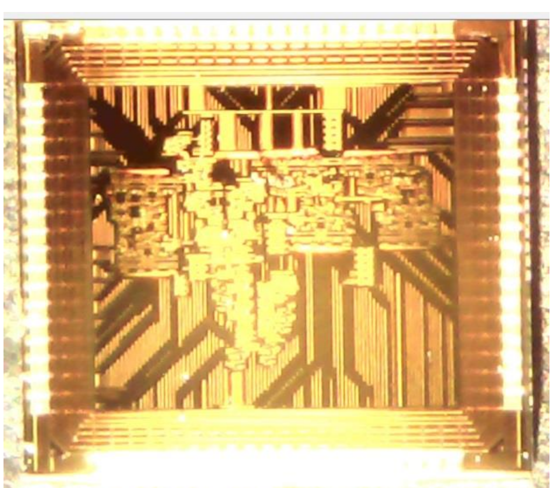


Fig. 3: Phase Shifter – naked chip

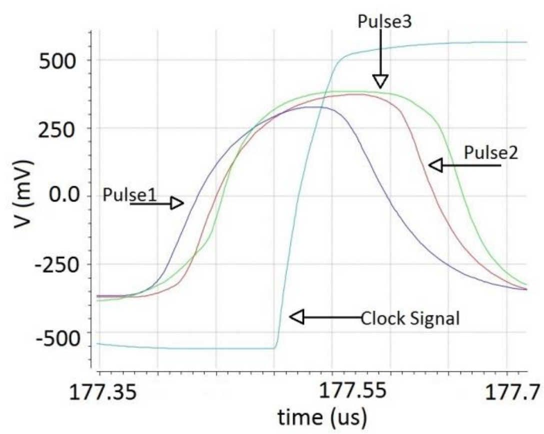
III. SIMULATIONS

The PCB has been simulated by using the layout with parasitic extraction for the chip. The clock frequency has been imposed to 2 GHz so the chip can provides 1024 phased square waves with a minimum phase shift of 0.3515° that correspond to 0.5 ns in time domain. The frequency of these waves is 1.953MHz in accord to equation (1).

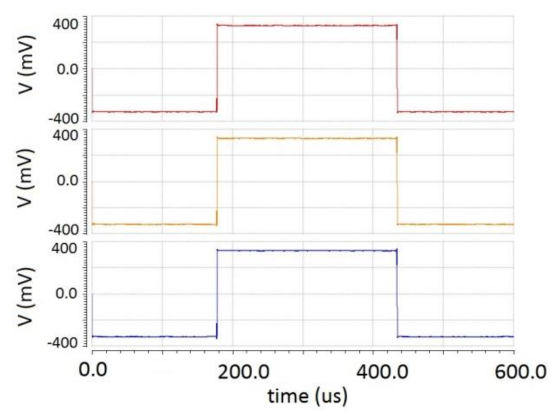
The first step was to verify the synchronism of the channels, that is, when the same phase word is imposed for all the channels. In Fig. 4 a phase word equal to 0100000000b has been imposed. Fig 4a shows the output comparator, where blue line is the clock signal used to align the phased square waves depicted in Fig. 4b, where it can be noticed the perfect alignment of the output waves. .

After verifying that the internal propagation delay does not affect the phase shift operation, the first channel has been considered as the reference channel and the 1024 relative phase shifts have been simulated for the other two channels.

A sub-set of the results of these simulations is summarized in Table I, where are listed the MSB period, TMSB, the ideal time delay, TDi, the simulated time delay, TDs, and the phase shift, ΔΦ. The results demonstrate that the PCB can produce phase-shifted square waves with a very high phase-shift precision. Indeed, the worst-case phase error is less than 0.008°.



(a)



b)

Fig. 4: Output signals of comparators – a) Pulses of phasing . b) Phased Square waves

Finally an example of phased waves is depicted in Fig. 5 where a 90° and 180° phase shift have been imposed for channel two and channel three respectively.

Table I

Phase Word	TMSB [ns]	TDs [ns]	TDi [ns]	$\Delta\phi$ [deg]
0	512	-	-	0
1	512	0.500	0.500	0.3516
2	512	1	1	0.7031
3	512	1.499	1.500	1.0548
7	512	3.500	3.500	2.4612
17	512	8.490	8.500	5.9772
31	512	15.498	15.500	10.8996
43	512	21.494	21.500	15.1188
401	512	200.500	200.500	140.9916
516	512	258.000	258.000	181.4256
1023	512	511.500	511.500	359.6868

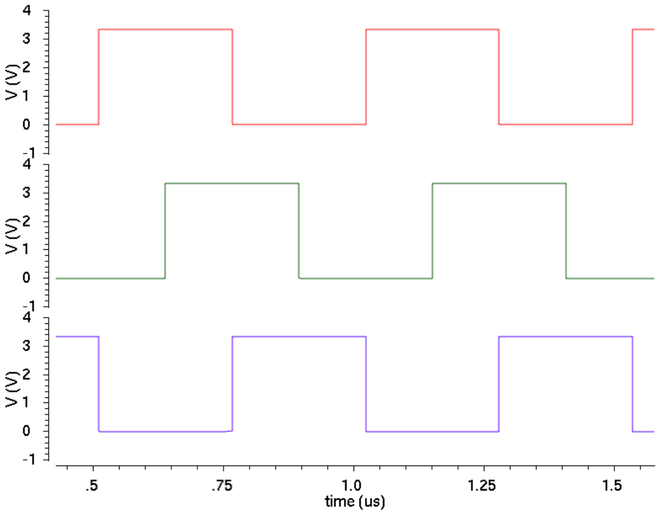


Fig. 5: PCB simulated output squared waves with 90° and 180° phase shift

IV. Prototype and Measurements

Two different prototypes have been realized. The first one is composed only by the IC fabricated and a microcontroller which imposes the phase words to the three channels. A direct comparison with the simulation results will be presented in the next sub-section.

The second prototype is composed by the IC fabricated, the microcontroller for the phase words setting and three PLLs with external VCO, in order to test the complete architecture.

A. *IC phase shifter and microcontroller*

In the first testbench a microcontroller provides the input phase word to the comparators of the phase control block. The external reference imposes the 2GHz clock frequency for the phase control block and it has been used an oscilloscope to measure the relative phase shifts between the channels.

Also in this case the first step was to verify the channels alignment and then to measure all the relative phase shifts.

In Fig. 6 the same phase word has been imposed for all the channels, while in Fig. 7 the same phase shift imposed as in Fig. 5 is shown.

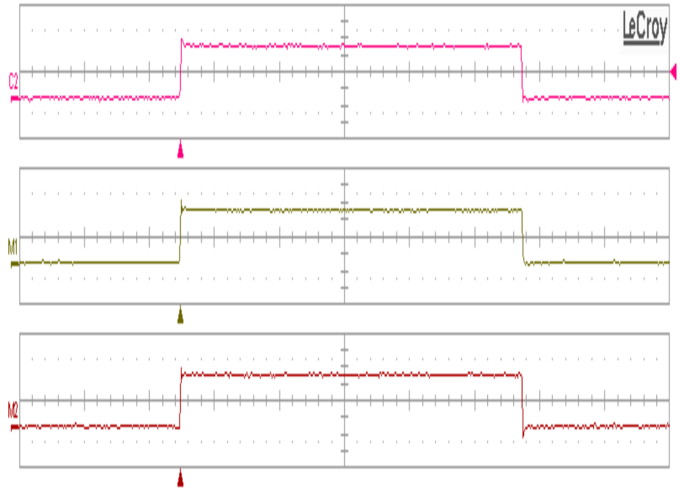


Fig. 6: PCB measured output waveforms with the same phase control word for all the three channel

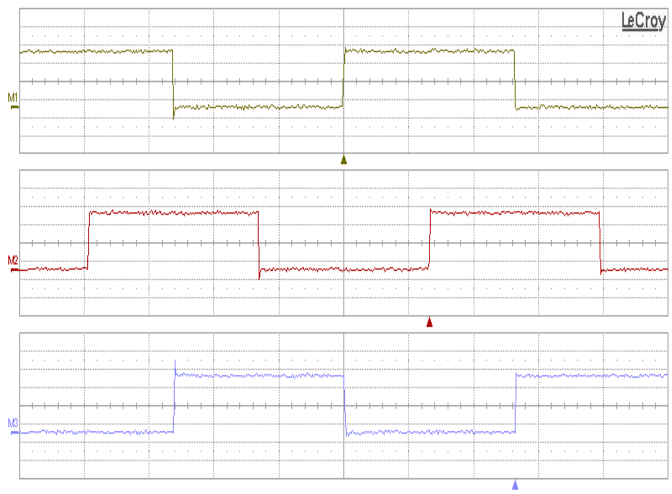


Fig. 7: PCB measured output squared waves with 90° and 180° phase shift

In general for the relative phase shift measurements, the first channel has been considered as the reference channel and the other two channels as the phased ones. In Fig. 8 there are represented the measured characteristics when a phase word equal to 0000000000b has been imposed for the channel 0.

It can be noticed the almost perfect overlap of the measured characteristics with the ideal one.

In Fig. 9 the phase error of the channel two and channel three is shown. The maximum phase error is about 0.1° for both the channels; the rms error is about 0.0585° for the second channel and 0.0588 for the third channel.

The measures were been repeated imposing the phase word to the reference channel equal to 1111100000b and the results are shown in Fig. 10. Also in this case the maximum error phase shift is about 0.1° and the rms error is about 0.0581° for the second channel and 0.0592 for the third channel.

These tests confirm perfectly the simulations results.

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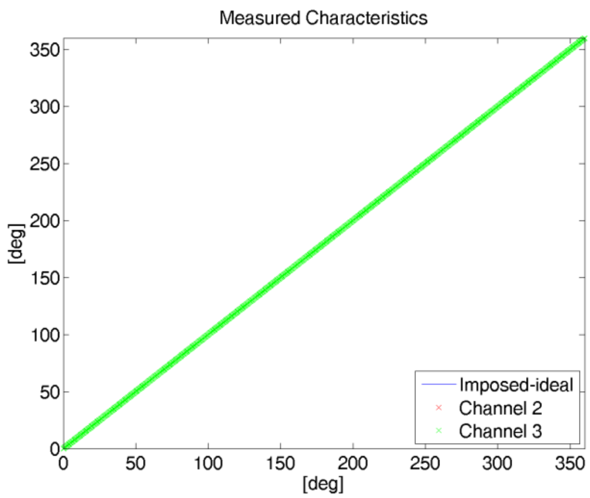
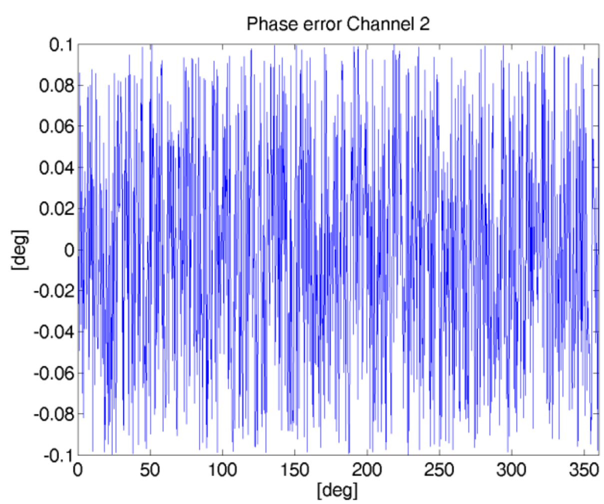


Fig. 8: PCB measured output characteristic



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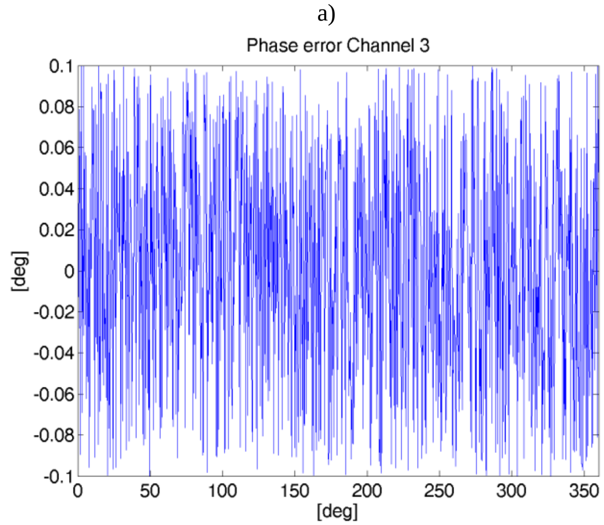
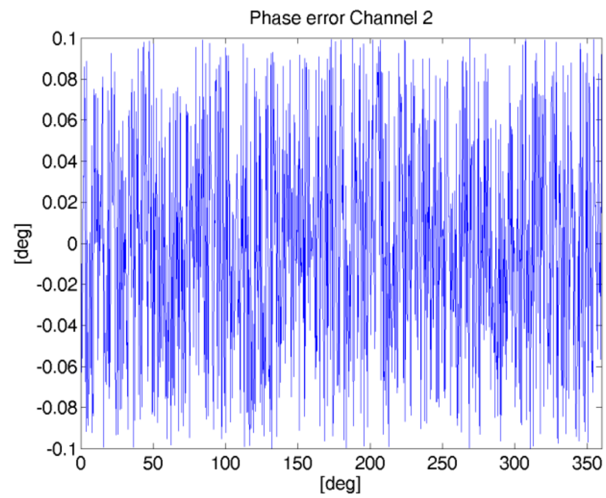
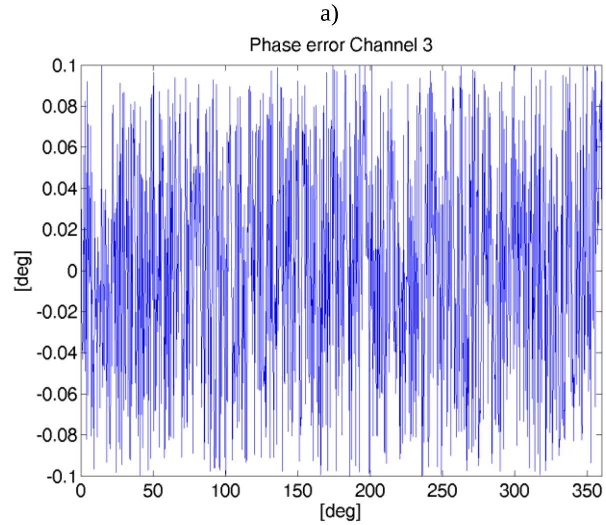


b)

Fig. 9: PCB phase shift error with phase control word equal to 0000000000b for the channel one. a) Channel two; b) channel three



a)



b)

Fig. 10: PCB phase shift error with phase control word equal to 1111100000b for the channel one. a) Channel two; b) channel three

B. IC phase shifter, microcontroller, PLL and VCO

In the second testbench, PLLs synthesize the desired output frequency without deteriorating the achievable good phase resolution. The VCO output frequency was set to 2.45GHz.

For uniformity the same tests previously made are reported. In Fig. 11 there are the output sinewave when the same phase word is imposed for all the three channels.

In Fig. 12 the same phase shifts imposed as in Fig. 5 are shown.

All the 1024 phase shifts have been measured for the center frequency.

As shown in Fig. 13 it can be noticed that the maximum phase error is increased and it is due to the phase noise introduced by the PLL and VCO. The rms phase error is equal to 0.0854° for the channel two and 0.866° for the channel three.

It demonstrates the validity of the proposed approach.

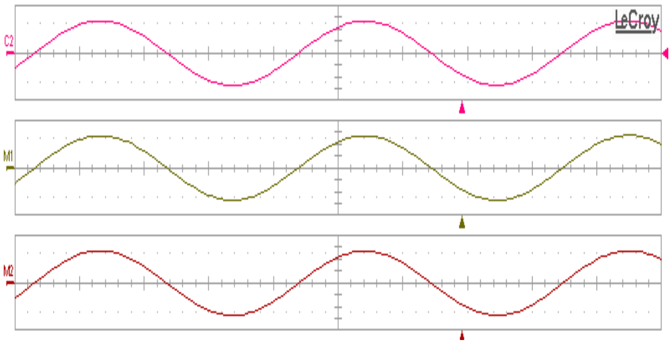


Fig. 11: VCO measured output waveforms with the same phase control word for all the three channel

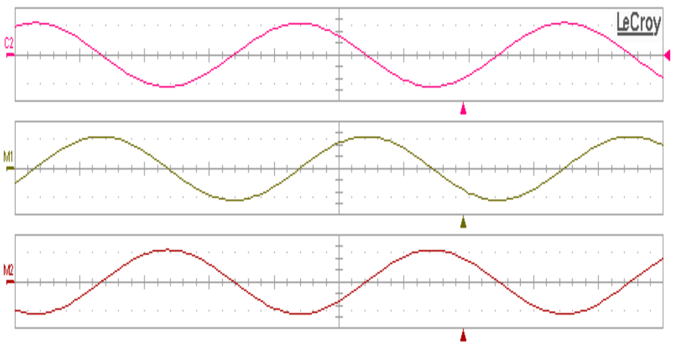
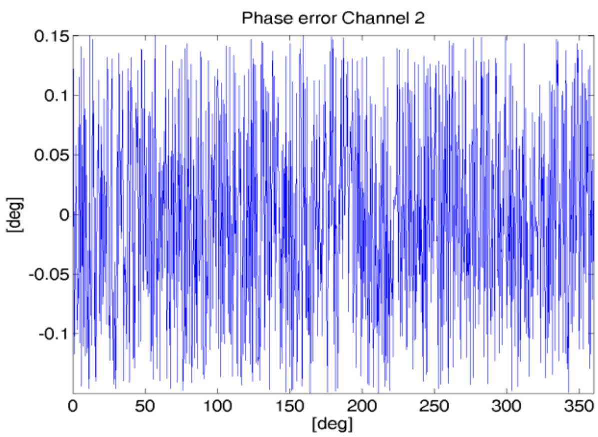
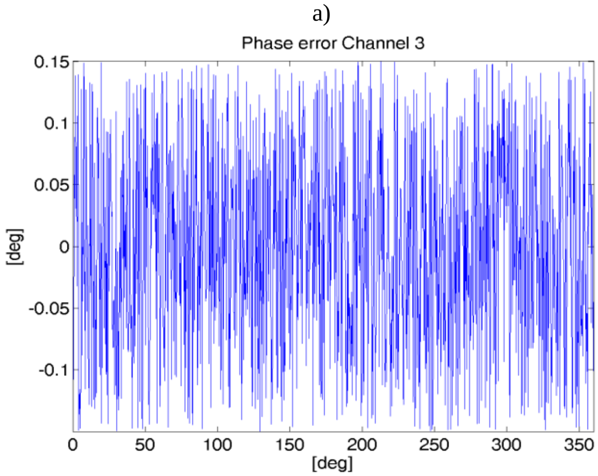


Fig. 12: VCO measured output waveforms with 90° and 180° phase shift



a)



b)

Fig. 9: VCO phase shift error with phase control word equal to 0000000000b for the channel one. a) Channel two; b) channel three

V. CONCLUSION

In this paper a high precision phase shifter has been presented. The system was realized in 0.35 µm SiGe BiCMOS process and allows generating phased square-waves with a minimum step of 0.3515°. The great flexibility of the proposed architecture is given by its frequency independency and scalability; in fact it is simply demanded at the use of suitable PLLs and VCOs while the phase resolution is demanded to a very simple digital circuit.

The PCB output signals have a maximum phase error of about 0.1° and an rms error equal to 0.0592°. A slight deterioration has been measured at 2.45GHz where the maximum phase error is about 0.15° and the rms error is about 0.0866°.

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Design of High performance and Low Power 16T Full Adder Cells for Subthreshold Voltage Technology

Ebrahim Pakniyat, Seyyed Reza Talebiyan

Abstract— This paper presents two new structures of 1-bit full adder. It compares full adder sub-circuits and two proposed full adder circuits with common circuits in terms of propagation delay, power consumption, PDP, and P^2DP in subthreshold voltage technology. HSPICE simulations show that all the proposed adders are improved significantly in PDP and P^2DP parameters. The full adder structures are compared in 260 (mV) voltage source.

Keywords—1-bit adder, subthreshold voltage technology, propagation delay, power consumption, performance.

I. Introduction

ADDERS are usually the most common cells used in digital systems. For instance, these circuits may be applied in Arithmetic circuits and DSP systems. Power consumption and Delay time are two important parameters that must be decreased simultaneously. Power consumption is important more than Delay time, specially for portable devices. Designing adder circuits in subthreshold voltage is a suitable method for considerable reduction of power consumption [1]. In designing circuits at subthreshold voltage, a source voltage should reduce gradually as much as the threshold voltage. Power reduces considerably in the implemented circuits merely through the subthreshold current, which is achieved by correct regulation of circuit voltage source (V_{dd}) lower or equal to the threshold voltage (V_{th}). The current of transistors at subthreshold voltage is related exponentially to gate voltage, which reduces power consumption exponentially and increases delay in the circuit [1]. Consequently, a VLSI designer should use a kind of trade-off between Delay time and Power consumption. A comparison can be made with respect to circuits' PDP to compensate for the parameters. In fact, this article aim at examining performance of these structures using supply voltage reduction. Of course, this paper defined P^2DP for making a better comparison and showing power consumption importance at low voltages. Section 2 introduces design of full adders. Section 3 demonstrates circuits of the three full adder modules. Section 4 discusses simulation to select a superior structure and to present the results. Section 5 presents an overall conclusion on the activities performed in this paper.

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II. Design Full adder

Figure (1) shows the diagram of an XOR-XNOR-based 1-bit full adder. The circuit consists of three major modules. Since the modules may be implemented using various methods and logics, a full adder circuit can be designed using different forms and logics. In this figure, A and B are the inputs, C_{in} is the carry input, and Sum is total and C_{out} is the output carry. Expressions (1) and (2) present the relationship between the inputs and outputs [2].

$$S = A \oplus B \oplus C_{in} \tag{1}$$

$$C_{out} = A.B + A.C_{in} + B.C_{in} \tag{2}$$

The Boolean expression in (1) and (2) may be arranged by the following expressions.

$$H = A \oplus B \tag{3}$$

$$Sum = H \oplus C_{in} = H.\overline{C_{in}} + \overline{H}.C_{in} \tag{4}$$

$$C_{out} = A.\overline{H} + C_{in}.H \tag{5}$$

Expressions (4) and (5) show, H and its complement $\overline{H}$ are the preliminary variables for Sum and C_{out}, H and $\overline{H}$ should be produced in the module I, which are used in module II with C_{in} for creating C_{out}. Module III was used for producing C_{out} using H, $\overline{H}$, A, and C_{in} outputs [3]. According to the study of all full adders at subthreshold voltages, attempts were made here not to use NOT gates as much as possible to reduce power consumption whose major factor at low voltages is leakage power. Therefore, the circuits are used for module I, which create H and $\overline{H}$ signals simultaneously without needing a NOT gate. A NOT gate usually need for producing a $\overline{H}$ signal in XOR-XOR-based or XNOR-XNOR-based adder structures, at the following discusses XOR-XNOR-based adders.

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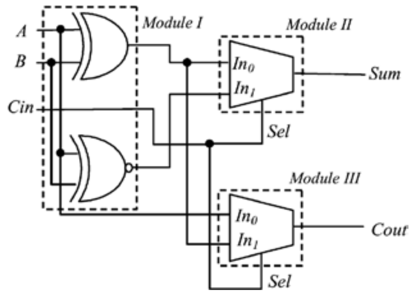

Fig. 1 general form of XOR–XNOR-based full adder [2].

Sum and Carry outputs are produced using expressions (4) and (5) in all the XOR-XNOR-based adders. In this full adder, module I includes an XOR-XNOR circuit that generates H and $\overline{H}$ signals. Modules II and III include, 2-to-1 multiplexers with select lines of H and $\overline{H}$, which generate sum and carry outputs, respectively. Simultaneous generation of H and $\overline{H}$ signals in full adders is important as they drive select lines of output stage of multiplexers. In another case (non-simultaneous H and $\overline{H}$), there may be glitches and unnecessary power dissipation may occur. The final outputs cannot be generated until these intermediate signals are available from module I.

At section III discusses the circuits that have presented for the three full adder's modules.

III. Full Adder building blocks

XOR and XNOR gates play a crucial role in different circuits, especially computational circuits and their optimal design improves efficiency of the circuits. According to the importance of designing and manufacturing full adders, it is necessary to discuss XOR and XNOR circuits design because they have been considered as the most fundamental element in designing this level of circuits. Simultaneous generation of XOR and XNOR has been used recently for module I extensively [4, 5]. This feature is extremely favorable as output signals are generated in the module for driving select lines of a multiplexer in a full adder. Figure (3) shows all the circuits that have been designed already for module I.

Figure (4) shows some frequently used circuits that have been presented already for module II. The circuits necessarily perform XOR or XNOR and they can be used in adder module I; however, they cannot have an appropriate performance in that module.

Figure (2) shows the 2-to-1 multiplexer circuit for module III. Output of the module can be expressed as expression (5).

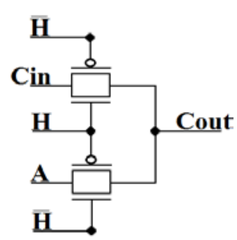

Fig. 2 circuit for module III [2]

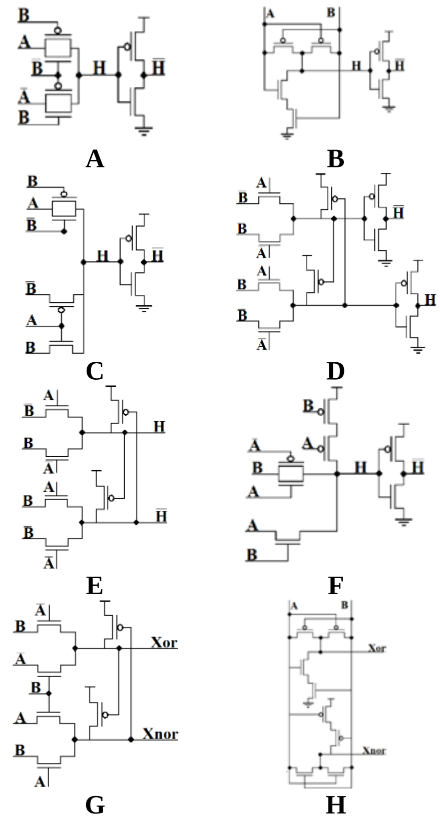

Fig. 3 circuit for module I [2]

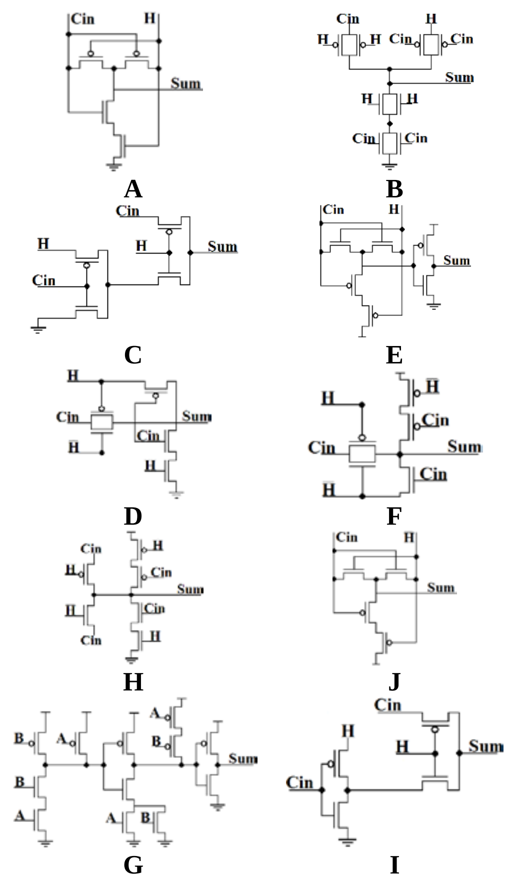

Fig. 4 circuit for module II

IV. HSPICE Simulation and Results

HSPICE and 90 nm PTM library were employed here for performing simulations. V_{DD}=1.2V was used for nominal value of the voltage source. The results were presented for module I and module II in voltage sources of V_{DD}=220mV and V_{DD}=310mV, respectively. V_{DD}=260mV voltage source was used for comparing the full adders. Input and output buffers were used for all inputs and outputs to simulate a real environment. Figure (5) shows the test structure for general simulation and size of transistors in each buffer. Size of transistors of these buffers is selected in a way that there is sufficient expected signal distortion in a real circuit.

Inputs of a 1-bit full adder (A, B, and C_{in}) may change into 56 different modes. That is, three inputs of a 1-bit adder may represent eight binary figures as "000" to "111". Each eight binary figures ("000" to "111") should spring into all figures except itself. Therefore, there are seven springs for each eight binary figures. Consequently, all possible mode changes equal $8\times 7=56$. This method was used for simulation of all modules. Performances of the full adder circuits and the proposed modules were evaluated in terms of the worst delay mode, power consumption, PDP, P^2DP, in 1MHz frequency. The delay is calculated from 50% of the input voltage level to 50% of the output voltage level obtained from all the rising and falling output transitions. In order to calculate the delay in the worst condition, all the 56 modes should be examined to measure the delay of all output mode changes (C_{out} and Sum) and introduce the biggest delay as the worst delay [2]. To have an identical comparison, all full adder circuits and simulated blocks were sized with the optimal size of the transistor.

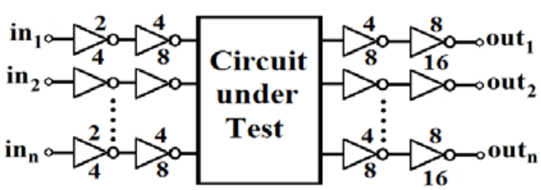

Fig. 5 simulation test bench

Tables (1) and (2) show the simulation results related to studying the circuits shown for module I and module II, such as of delay, power consumption, PDP, and P^2DP.

Table 1. Module I HSPICE simulation results at 90nm, V_{DD}=220mV

Circuit	No. of Tr.	Power (nW)	Delay (nS) Xor	Delay (nS) Xnor	PDP (aJ)	P^2DP
A	10	13.56	9.39	12.09	164.06	2.225
B	6	12.39	9.20	16.02	198.51	2.459
C	8	13	9.18	12.16	158.17	2.056
D	14	14.89	10.88	9.69	162.07	2.413
E	10	13.84	7.77	8.22	113.9	1.576
F	9	13.14	11.88	9.01	156.2	2.053
G	8	13.30	11.08	13.39	178.2	2.372
H	8	13	10.13	7.762	131.8	1.714

Table 2. Module II HSPICE simulation results at 90nm,V_{DD}=310mV.

Circuit	No. of Tr.	Power (nW)	Delay (nS)	PDP (aJ)	P^2DP
A	4	13.823	2.219	30.68	4.240
B	8	14.253	2.076	29.59	4.217
C	4	13.053	3.139	40.97	5.348
D	5	9.611	11.506	110.58	1.062
E	6	14.884	3.136	46.68	6.948
F	4	9.4007	10.287	96.706	0.909
G	12	16.728	5.880	98.36	16.453
H	6	9.752	11.33	110.51	1.077
I	4	15.042	3.006	45.22	6.802

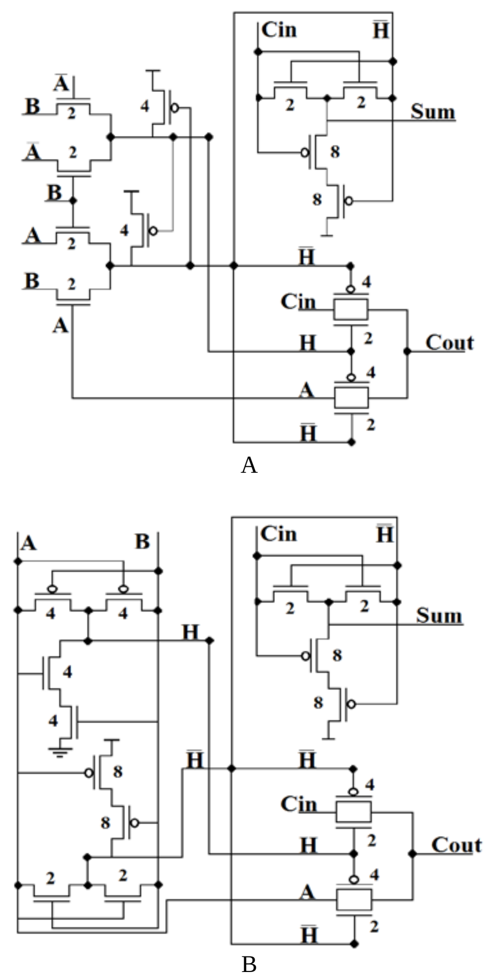

Fig. 6 Proposed 1bit-full adder circuits, (A. Proposed Circuit-1, B. Proposed Circuit-2).

J	4	13.96	2.058	28.73	4.011

Table 3. Full adder HSPICE simulation results at 90nm, V_{DD}=260mV

Full Adder	No. of Tr.	Power (nW)	Delay(nS)		PDP (aJ)	P^2DP
			Sum	Cout		
14T	14	-	-	-	-	-
CMOS	28	24.14	15.80	9.52	381.6	9.21
Hybrid CMOS	24	24.43	16.14	12.39	394.5	9.64
Hybrid	26	24.88	13.70	16.45	409.3	10.18
HPSC	22	24.44	25.57	13.74	599.6	14.06
DPL	28	24.29	12.07	11.65	293.1	7.12
TG	20	22.62	11.71	9.14	264.9	5.99
CPL	28	26.17	9.68	10.23	267.9	7.01
SRCPL	24	24.01	9.46	10.03	240.8	5.78
Full Adder in [2]	24	24.436	16.14	12.39	394.5	9.64
Full Adder in [8]	19	22.107	16.44	10.96	363.6	8.03
Full Adder in [7]	18	21.55	14.96	10.26	322.5	9.95
Full Adder in [6]	16	24.78	13.21	11.91	327.4	8.11
Proposed Circuit-1	16	21.55	10.38	10.18	223.8	4.82
Proposed Circuit-2	16	21.13	10.11	8.81	213.8	4.51

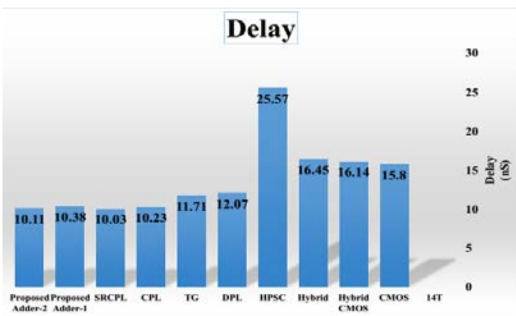

Fig. 7 Simulation results of Delay for the compared full adders

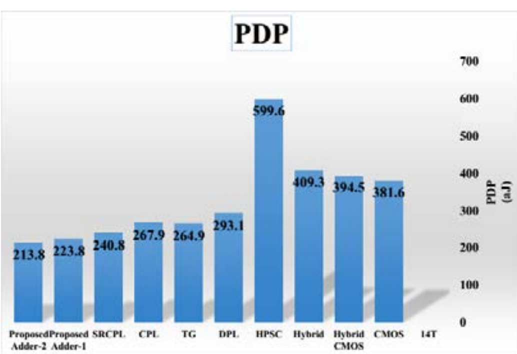

Fig. 8 Simulation results of PDP for the compared full adders

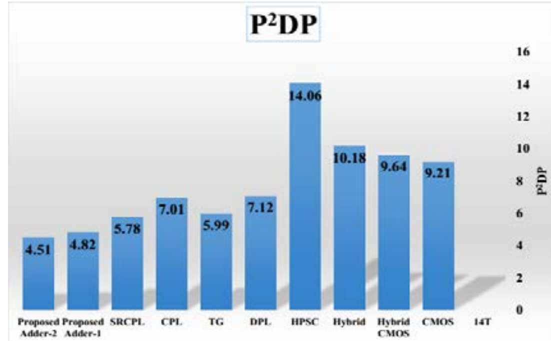

Fig. 9 Simulation results of P^2DP for the compared full adders

Fig. 10 Simulation results of Power consumption for the compared full adders

The results show that circuits G and H is the superior structures of module I, F and J circuits are the superior structures for module II. Figure (6) shows the two new structures of full adders, which were designed using the modules.

Table (3) shows the simulation results of the common full adders and the two proposed full adders such as number of transistors, delay, power consumption, PDP and P^2DP. Figures (7) to (10) exhibit a comparison of Table (3) results by a diagram.

V. CONCLUSION

This paper presents two new full-adder circuits suitable for subthreshold voltage technology.

These new structure are obtained by selection of the best circuits of module I & module II (the basic building blocks of full-adder circuit). These new circuits show 11.2% and 7.05% improvements in PDP at worst case mode.

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Design of New Low-Power High-Performance Full Adder Cell Using Hybrid-CMOS Logic Style

Milad Jalalian, Seyed Reza Talebiyan, Ebrahim Pakniyat

***Abstract*—**In this paper, we present a new design for a 1-bit full adder using hybrid-CMOS logic style. The new full adder cell has been formed by a few number of transistors and offers lower power consumption and power-delay product (PDP) than standard implementations of the 1-bit full adder cell. In proposed full adder cell, the short-circuit component of power consumption is low, because of using only one CMOS-inverter in this. This circuit outperforms its counterparts showing 5%-46% and 10%-46% improvement in PDP and power consumption, respectively. HSpice simulations using 90nm technology with a power supply of 1.2V was utilized to evaluate the performance of the circuits.

***Keywords*—**Full adder, high-performance, hybrid-CMOS, Low-power.

I. Introduction

MOST of the VLSI applications, such as digital signal processing, image processing, and digital filter design, widely use arithmetic operations. Addition, subtraction and multiplication are examples of the most commonly used operations. The 1-bit full adder cell is the building block of these units. Hence, improving its performance is critical for improving the overall unit performance. The most important performance parameters for a generic VLSI system are power consumption, speed, and chip area.

Several logic styles have been used in the past to design full adder cells. Each logic style has its own advantages and disadvantages. Classical designs of full adders normally used only one logic style for the whole full adder design. Standard static CMOS, members of pass-transistor logic (PTL) family such as CPL, DPL, SRPL, and transmission gate are the most important logic styles in the conventional full adders [1]. In the other full adder designs, more than one logic style have been used. These designs are called hybrid-CMOS logic style [2]. These designs use the features of different logic styles to improve upon the performance of the designs using single logic style. HPSC full adder (hybrid pass logic with static CMOS output drive full adder) [3], and new-hybrid-CMOS adder [4], are the examples of adders designed with this logic style. In this paper, we propose a novel 1-bit full adder with better power consumption and PDP in comparison with conventional CMOS, CPL, HPSC and new-hybrid-CMOS full adders.

The authors are with the Electrical Engineering Department, Imam Reza International University, Mashhad, Iran (e-mail: jalalian.milad@gmail.com; talebiyan@imamreza.ac.ir; e.pakniyat@imamreza.ac.ir).

The rest of this paper is organized as follow, in section II, power consumption issues in CMOS VLSI circuits will be discussed. In section III, the main structure of a 1-bit full adder will be introduced. Then in section IV, we present the new 1-bit full adder cell. In section V, simulation environment will be described and in section VI we propose the simulation results, which show the supremacy of the proposed cell. Finally, in section VII, we conclude the paper.

II. Power Consumption in VLSI circuits

There are three main components of power consumption in digital VLSI circuits.

1) *Switching component:* consumed in charging and discharging of the circuit capacitances during transistor switching.
2) *Short-circuit component:* Created by short-circuit current flowing from supply voltage to ground during transistor switching.
3) *Static power component:* Existence of static and leakage currents in stable state of circuit cause this component of power consumption.

The first two components are referred to as dynamic power, since power is consumed dynamically while the circuit is changing states [5]. Dynamic power accounts for the majority of the total power consumption in digital VLSI circuits [6]. It depends on the input pattern applied to the circuit, which will either cause the transistors to switch or to keep their previous state at each clock cycle [5]. The third component is usually negligible in a well-designed CMOS circuit [6].

The total power is given by

$$P_{total} = V_{dd}.f_{clk}.\sum_i V_{swing}.C_{load}.p_i + V_{dd}.\sum_i I_{i\ sc} + V_{dd}.I_l \qquad (1)$$

where V_{dd} is the supply voltage. V_{swing} is the voltage swing of the output which is ideally equal to V_{dd}. C_{load} is the load capacitance at node i. f_{clk} is the system clock frequency. p_i is the switching activity at node i. I_{i-sc} is the short-circuit current at node i and I_l is the leakage current [5].

In this paper, low power consumption is targeted at the circuit level. Reducing the number and magnitude of the circuit capacitances, reducing the voltage swing at some internal nodes, and reducing the spurious transitions in the output signal are some of techniques used at the circuit level to reduce the power consumption [5].

III. Main Structure of 1-bit Full Adder

Generally, hybrid-CMOS full adders are categorized in three groups depending on their structure and logical expression of *Sum* output [4]. The first category of full adders is based on XOR gates and second one is based on XNOR gates. In third category, the *Sum* and *Carry* outputs are generated by XOR-XNOR intermediate signals [2]. In this paper, the proposed full adder stand on third category.

The *Sum* and *Carry* (C_{out}) outputs of a 1-bit full adder generated from the binary inputs A, B, and C_{in} can be generally expressed as

$$SUM = A \oplus B \oplus C_{in} \tag{2}$$

$$C_{out} = A.B + C_{in}\left(A \oplus B\right) \tag{3}$$

In third category, the Sum and Carry outputs are generated by the following expression, where H is the XOR of A and B, and H' is the complement of H

$$SUM = H \oplus C_{in} = H.C'_{in} + H'.C_{in} \tag{4}$$

$$C_{out} = B.H' + C_{in}.H \tag{5}$$

Generally, this category is divided by three modules. Module I is a XOR-XNOR circuit producing H and H' signals. Module II and III produce Sum and C_{out} as outputs, respectively. Module II and III are 2-to-1 multiplexers with H and H' as select lines. The simultaneous generation of H and H' signals is critical in these types of adders, because they drive the select lines of the multiplexers in the output stage. Otherwise, there may be glitches and unnecessary power dissipation may be occur [2]. The most common structures of full adders are shown in Fig. 1 to Fig. 4.

IV. Proposed Full Adder

The main structure of 1-bit full adder introduced in section III. As mentioned in the previous section, the proposed full adder stand on third category. It is shown in Fig. 5. The intermediate signals H and H' are produced by module I. module II generates the XNOR of H and C_{in} , then the *Sum* output signal is produced by inverting this signal. Module III is a multiplexer with H and H' as select lines, and produces the *Carry* output signal.

V. Description of Simulation Environment

HSpice simulations using 90nm technology with a power supply of 1.2V was utilized to evaluate the performance of the five circuits. To simulate a real environment, input buffers for all inputs of the test circuit are used. The transistor sizes of these buffers are chosen such that there is sufficient signal distortion as expected in an actual circuit. A minimum output load of fan-out of four inverters (FO4) is used for power and delay measurements [4], the value of which amounts to 2.656fF (0.664fF for each inverter in 90nm technology).

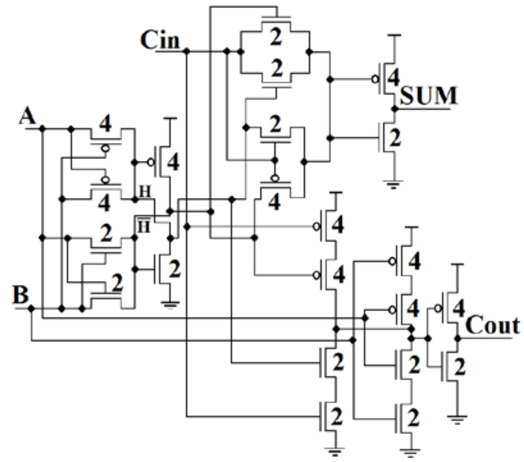

Fig. 1 HPSC full adder cell

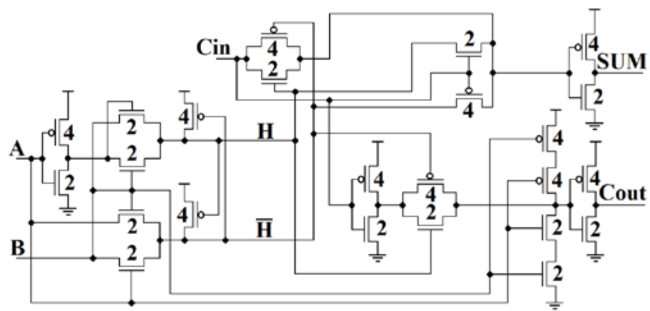

Fig. 2 New-hybrid-CMOS full adder cell

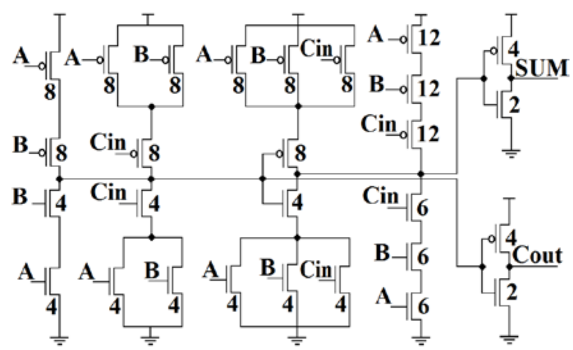

Fig. 3 Conventional static CMOS full adder cell

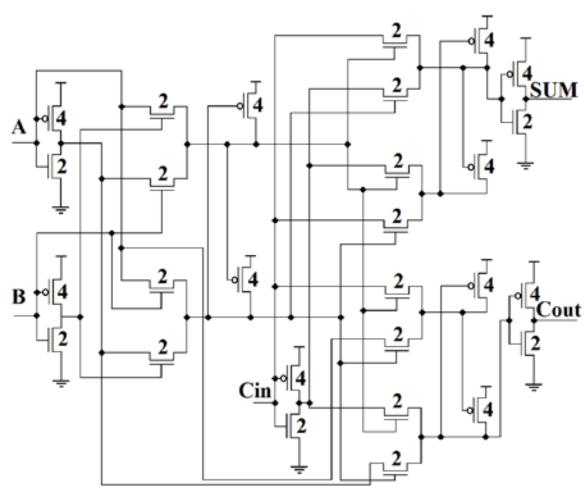

Fig. 4 CPL full adder cell

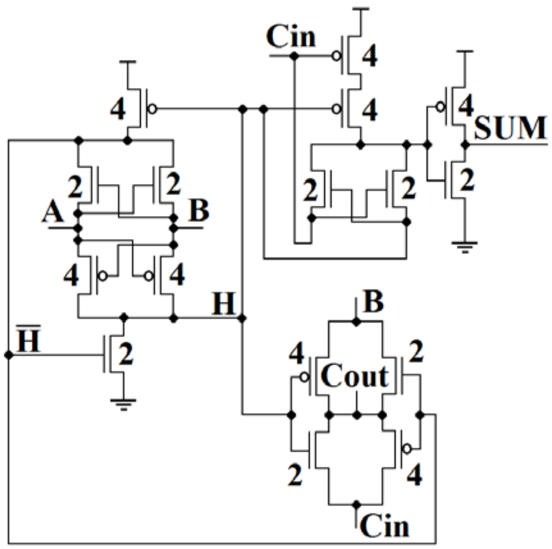

Fig. 5 Proposed full adder cell

The generic simulation test bench used is shown in Fig. 6 along with the transistor sizes of each buffer. To reach more accurate results, all transitions from an input combination to another (56 patterns) have been tested, and the delay at each transition has been measured. The maximum has been reported as the cell delay. Fig. 7 shows the output signals and input stimulus used for the full adder circuits. The average power for the duration of this pattern has been reported as the cell power consumption figure. The transistor sizes of all the simulated circuits have been included in the figures. In the circuits, the numbers depict the width (W) of the transistors with the minimum feature size as 2λ.

VI. Simulation Results

In this section, simulation of full adder cells is presented under the mentioned conditions in previous section. The circuit performance of the test circuits is evaluated in terms of worst-case delay, power dissipation, and power-delay product at 1.2V supply voltage. The simulation results are shown in Table I. According to the results, the proposed full adder is the best structure in terms of power consumption and power-delay product (energy). The proposed full adder consumes 10% less power than HPSC, 23% less than conventional static CMOS, 25% less than new-hybrid-CMOS and 46% less than CPL.

In addition the power-delay product of proposed full adder is 5% better than conventional static CMOS, 6% better than CPL, 15% better than HPSC and 46% better than new-hybrid-CMOS. The number of transistor in the proposed cell (16 transistors) is the other advantage of this over its counterparts. Moreover, the simulation results for power consumption and PDP have been depicted in the column chart in Fig. 8 and 9, respectively.

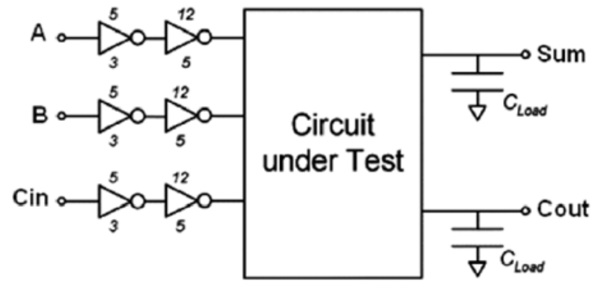

Fig. 6 Simulation test bench

TABLE I
Simulation Result for the Five 1-Bit Full Adder Cells

FA	HPSC	New hybrid CMOS	Conventional CMOS	CPL	Proposed
No of Tr.	22	24	28	28	16
Power (nW)	228.07	258.33	253.97	303.03	207.11
Delay (pS)	135.61	152.71	111.18	94.678	130.21
PDP (e-18)	30.93	39.45	28.24	28.69	26.97

VII. Conclusion

A novel low-power 1-bit full adder has been proposed. Low power consumption is targeted at the circuit-design level. The cell is characterized by only one inverter, so the short-circuit component of power consumption is low. The simulation result indicated that the proposed full adder has minimum power consumption and PDP compared to its counterparts.

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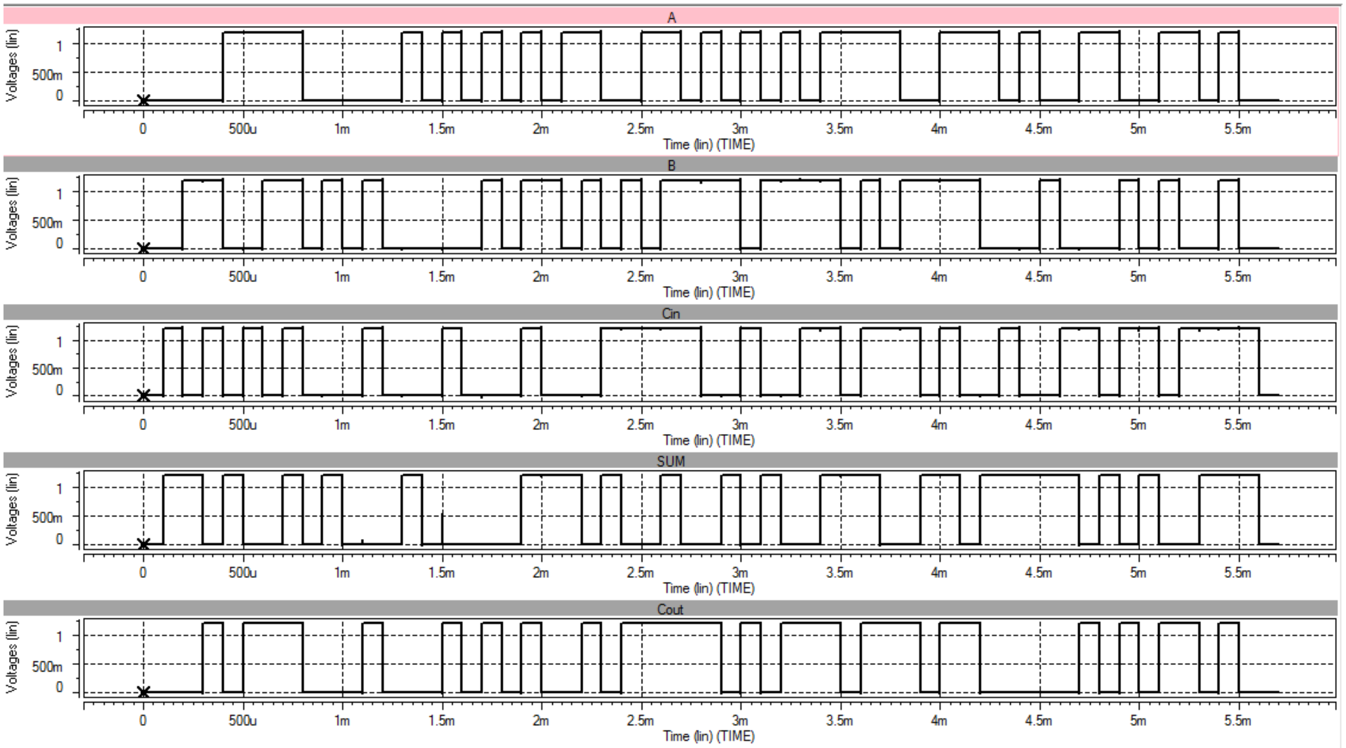

Fig. 7 Input stimulus used for the full adder circuits and output signals

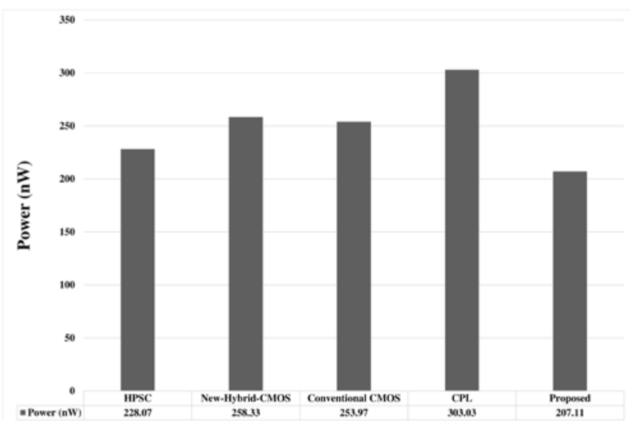

Fig. 8 Simulation results for power consumption

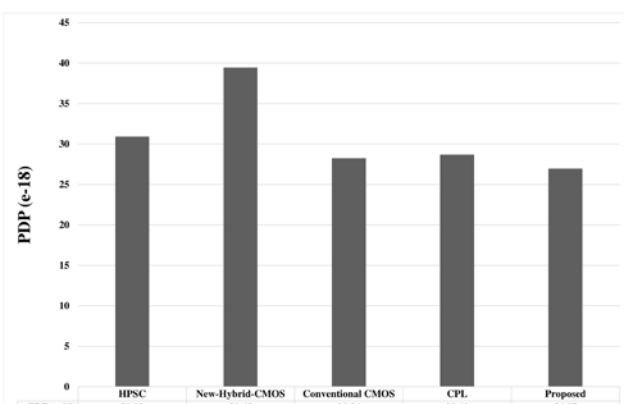

Fig. 9 Simulation results for power-delay product (PDP)

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Influence of Parametric Uncertainties on Control Quality of Time-delay Processes

V. Bobál, P. Dostál, and M. Kubalčík

Abstract**—**Time-delays are mainly caused by the time required to transport mass, energy or information, but they can also be caused by processing time or accumulation. Typical examples of such processes are e.g. pumps, liquid storing tanks, distillation columns or some types of chemical reactors. This paper deals with a design of a universal and robust digital control algorithms for control of great deal processes with time-delay. These algorithms are realized using the digital Smith Predictor (SP) based on polynomial approach – by minimization of the Linear Quadratic (LQ) criterion. For minimization of the LQ criterion is used spectral factorization principle with application of the MATLAB Polynomial Toolbox. The designed polynomial digital Smith Predictors were verified in simulation conditions. The main contribution of this paper is an experimental simulation examination of the robustness of the designed control algorithms. The program system MATLAB/SIMULINK was used for this purpose.

Keywords**—**Digital LQ control, Polynomial approach, Smith Predictor, Time-delay, Robustness.

I. Introduction

TIME-delay may be defined as the time interval between the start of an event at one point in a system and its resulting action at another point in the system. Delays are also known as transport lags or dead times; they arise in physical, chemical, biological and economic systems, as well as in the process of measurement and computation. One older classification of techniques for the compensation of time-delayed processes is introduced in [1, 2] and newer overview of recent advances and open problems it is possible to find in [3].

The existence of pure time lag, regardless if it is present in the control or/and the state, may cause undesirable system transient response, or even instability. Consequently, the problem of controllability, observability, robustness, optimization, adaptive control, pole placement and particularly stability and robust stabilization for this class of systems, has been one of the main interests for many scientists and researchers during the last five decades. It is possible to say in present (see e. g. [4]) that "The beginning of the 21st century can be characterized as the *time-delay boom* leading to numerous important results".

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When a high performance of the control process is desired or the relative time-delay is very large, a predictive control strategy is one possible approaches for a control of time-delay processes. The predictive control strategy includes a model of the process in the structure of the controller. The first time-delay compensation algorithm was proposed by Smith [5] in 1957. This time-delay compensator (TDC) known as the Smith Predictor (SP) contained a dynamic model of the process and it can be considered as the first model predictive algorithm.

Historically, first modifications of time-delay algorithms were proposed for continuous-time (analog) controllers. In industrial practice the implementation of the time-delay compensators on continuous-time technique was difficult. Therefore the Smith Predictors and its modified versions can be implemented since 1980s together with the use of microprocessors in the industrial controllers. In spite of the fact that these algorithms can be implemented in digital platforms, most of the literature analysis and synthesis time-delay systems including the robustness, disturbance rejection and the extension of suitable compensators, is focused only in the continuous-time version. The first digital time-delay compensators are presented (see e.g. in [6]).

One of possible approaches to control of processes with time-delay is digital Smith Predictor based on polynomial theory. Polynomial methods are design techniques for complex systems (including multivariable), signals and processes encountered in Control, Communications and Computing that are based on manipulations and equations with polynomials, polynomial matrices and similar objects. Systems are described by input-output relations in fractional form and processed using algebraic methodology and tools. The design procedure is thus reduced to algebraic polynomial equations [7]. Controller design consists in solving polynomial (Diophantine) equations. The Diophantine equations can be solved using the uncertain coefficient method – which is based on comparing coefficients of the same power. This is transformed into a system of linear algebraic equations [8]. Because the classical analog Smith Predictor is not suitable for control of unstable and integrating time-delay processes, the polynomial digital LQ Smith Predictor for control of unstable and integrating time-delay processes has been designed in [9].

It is obvious that the majority processes met in industrial practice are influenced by uncertainties. The uncertainties suppression can be solved either implementation adaptive control or robust control. Some adaptive (self-tuning) modifications of the digital Smith Predictors are designed in [10] – [12]. Two versions of these controllers were implemented into MATLAB/SIMULINK Toolbox [13], [14].

Until recently, robust control and adaptive control have been viewed as two control techniques which are used for controller design in the presence of process model uncertainty (process model variations) [15].

The aim of this paper is the experimental examination of the robustness of control time-delay processes. Robustness is the property when the dynamic response of control closed loop (including stability of course) is satisfactory not only for the nominal process transfer function used for design but also for the entire (perturbed) class of transfer functions that express uncertainty of the designer about dynamic environment in which real controller is expected to operate. The design of robust digital controllers for systems with time delay is investigated in [16]. A particular class of digital controller is considered, namely based on the pole assignment approach.

The paper is organized in the following way. The general problem of a control of the time-delay systems with regard to robustness is described in Section I. The fundamental principle of digital Smith Predictor is described in Section II. Two versions of the primary polynomial LQ controller, which are components of the digital Smith Predictor, are proposed in Section III. The simulation verification of individual control-loops with their results are presented in Section IV. Section V. concludes this paper.

II. Principle of Digital Smith Predictor

The discrete versions of the SP and its modifications are more suitable for time-delay compensation in industrial practice. The block diagram of a digital SP (see [10], [11]) is shown in Fig. 1. The function of the digital version is similar to the classical analog version.

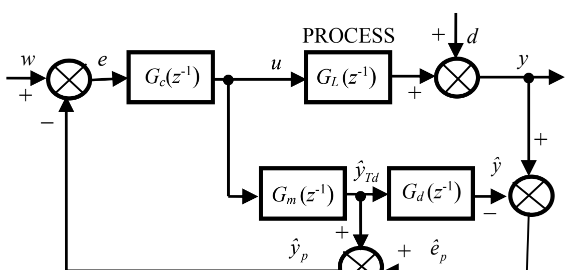

Fig. 1 Block diagram of a digital Smith Predictor

Number of higher order industrial processes can be approximated by a reduced order model with a pure time-delay. In this paper the following second-order linear model with a time-delay is considered

$$G_L\left(z^{-1}\right)=\frac{B\left(z^{-1}\right)}{A\left(z^{-1}\right)}z^{-d}=\frac{b_1z^{-1}+b_2z^{-2}}{1+a_1z^{-1}+a_2z^{-2}}z^{-d} \tag{1}$$

The term z^{-d} represents the pure discrete time-delay. The time-delay is equal to dT_0 where T_0 is the sampling period.

The blocks $G_m(z^{-1})$ and $G_d(z^{-1})$ are compensators. The difference between the output of the process y and the model including time-delay $\hat{y}$ is the predicted error $\hat{e}_p$ as shown in Fig. 1, whereas e and d are the error and the measured disturbance, w is the reference signal. The primary (main) controller $G_c(z^{-1})$ can be designed by different approaches (for example digital PID control or methods based on polynomial approach). The outward feedback-loop through the block in Fig. 1 is used to compensate load disturbances and modelling errors.

III. Design of Primary Polynomial 2DOF Controller

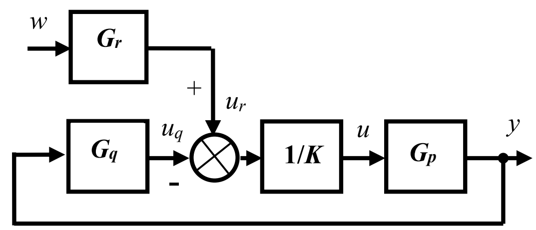

Fig. 2 Block diagram of a closed loop 2DOF control system

Polynomial control theory is based on the apparatus and methods of linear algebra. The design of the controller algorithm is based on the general block scheme of a closed-loop with two degrees of freedom (2DOF) according to Fig. 2.

The controlled process is given by the transfer function in the form

$$G_p(z^{-1})=\frac{Y(z)}{U(z)}=\frac{B(z^{-1})}{A(z^{-1})} \tag{2}$$

where A and B are the second order polynomials. The controller contains the feedback part G_q and the feedforward part G_r. Then the digital controllers can be expressed in the form of a discrete transfer functions

$$G_r\left(z^{-1}\right)=\frac{R\left(z^{-1}\right)}{P\left(z^{-1}\right)K\left(z^{-1}\right)} \tag{3}$$

$$G_q\left(z^{-1}\right)=\frac{Q\left(z^{-1}\right)}{P\left(z^{-1}\right)}=\frac{q_0+q_1z^{-1}+q_2z^{-2}}{\left(1+p_1z^{-1}\right)\left(1-z^{-1}\right)} \tag{4}$$

where $K\left(z^{-1}\right)=1-z^{-1}$.

According to the scheme presented in Fig. 2 and equations (2) – (4) it is possible to derive a polynomial Diophantine equation for computation of feedback controller parameters as coefficients of the polynomials Q and P

$$A(z^{-1})K(z^{-1})P(z^{-1})+B(z^{-1})Q(z^{-1})=D(z^{-1}) \tag{5}$$

where $D\left(z^{-1}\right)$ is the characteristic polynomial.

Asymptotic tracking of the reference signal w is provided by the feedforward part of the controller which is given by solution of the following polynomial Diophantine equation

$$S(z^{-1})D_w\left(z^{-1}\right)+B(z^{-1})R(z^{-1})=D(z^{-1}) \tag{6}$$

The 2DOF controller output is given by

$$u(k)=\frac{R\left(z^{-1}\right)}{K\left(z^{-1}\right)P\left(z^{-1}\right)}w(k)-\frac{Q\left(z^{-1}\right)}{K\left(z^{-1}\right)P\left(z^{-1}\right)}y(k) \tag{7}$$

Two primary polynomial LQ controllers are derived in this paper using minimization of LQ criterion [17]. For the minimization procedure is used spectral factorization by means of the MATLAB Polynomial Toolbox 3.0 [18].

A. Minimization of LQ Criterion Using Variable u(k)

In the first case the linear quadratic control methods try to minimize the quadratic criterion by penalization of the quadrat controller output $u(k)$

$$J=\sum_{k=0}^{\infty}\left\{\left[w(k)-y(k)\right]^2+q_u\left[u(k)\right]^2\right\} \tag{8}$$

where q_u is the so-called penalization constant, which gives the rate of the controller output on the value of the criterion (where the constant at the first element of the criterion is considered equal to one). In this paper, criterion minimization will be realized through the spectral factorization for an input-output description of the system

$$A(z)q_uA\left(z^{-1}\right)+B(z)B\left(z^{-1}\right)=D(z)\delta D\left(z^{-1}\right) \tag{9}$$

where δ is a constant chosen so that $d_0 = 1$.

Spectral factorization of polynomials of the first and the second degree can be computed simply by an analytical way [12], [19]; the procedure for higher degrees must be performed iteratively. Although $A(z^{-1})$ and $B(z^{-1})$ are the second degree polynomials (spectral factorization (9) can be computed by an analytical way), the MATLAB Polynomial Toolbox is used for this computation. The factorized polynomial $D(z^{-1})$ must be also of second degree

$$D_2\left(z^{-1}\right)=1+d_{21}z^{-1}+d_{22}z^{-2} \tag{10}$$

For computation of the spectral factorization (9) was used in this paper file *spf.m* by command

d = spf(a*qu*a' + b*b') (11)

It is obvious that by using of the spectral factorization, only two parameters d_{21} and d_{22} of the second degree polynomial $D_2(z^{-1})$ (10) can be computed. This approach is applicable only for control of processes without time-delay (out of Smith Predictor). The primary controller in the digital Smith Predictor structure requires usage of the fourth degree polynomial

$$D_4\left(z^{-1}\right)=1+d_1z^{-1}+d_2z^{-2}+d_3z^{-3}+d_4z^{-4} \tag{12}$$

in equations (5) and (6). The polynomial $D_2(z^{-1})$ (10) has two different real poles α, β or one complex conjugated pole $z_{1,2}=\alpha\pm j\beta$ (in the case of oscillatory systems). These poles must be included into polynomial $D_4(z^{-1})$ (12) and other two poles γ, λ are user-defined real poles. A suitable pole assignment was designed for both types of the processes in [9]. Then the primary 2DOF controller output is given by

$$\begin{aligned}u(k)&=r_0w(k)-q_0y(k)-q_1y(k-1)-q_2y(k-2)\\&+(1-p_1)u(k-1)+p_1u(k-2)\end{aligned} \tag{13}$$

where

$$r_0=\frac{1+d_1+d_2+d_3+d_4}{b_1+b_2} \tag{14}$$

and parameters q_0, q_1, q_2 are computed from (5).

B. Minimization of LQ Criterion Using Increment Δu(k)

In the second case the linear quadratic control methods try to minimize the quadratic criterion by penalization of the square incremental value of controller output $\Delta u(k)$

$$J=\sum_{k=0}^{\infty}\left\{\left[w(k)-y(k)\right]^2+q_u\left[\Delta u(k)\right]^2\right\} \tag{15}$$

Equation (9) for computation of the spectral factorization changes into

$$\begin{aligned}&(1-z)A(z)q_u\left(1-z^{-1}\right)A\left(z^{-1}\right)\\&+B(z)q_uB\left(z^{-1}\right)=D(z)\delta D\left(z^{-1}\right)\end{aligned} \tag{16}$$

It is obvious that after arrangement and substitution the first term of the left side (16) has this form

$$\left(1+a_{s1}z+a_{s2}z^2+a_{s3}z^3\right)q_u\left(1+a_{s1}z^{-1}+a_{s2}z^{-2}+a_{s3}z^{-3}\right) \tag{17}$$

where

$$A_s\left(z^{-1}\right)=1+a_{s1}z^{-1}+a_{s2}z^{-2}+a_{s3}z^{-3} \tag{18}$$

and

$$a_{s1} = a_1 - 1; \quad a_{s2} = a_2 - a_1; \quad a_{s3} = -a_3. \tag{19}$$

Because (18) is the third degree polynomial whose parameters and poles α, β and γ it is impossible to compute by an analytical way, MATLAB Polynomial Toolbox 3 was used for their computation using command (11).

The characteristic polynomial is the sixth degree polynomial in this case

$$D_6\left(z^{-1}\right) = 1 + d_1 z^{-1} + d_2 z^{-2} + d_3 z^{-3} + d_4 z^{-4} + d_5 z^{-5} + d_6 z^{-6} \tag{20}$$

Spectral factorization (16) gives three optimal parameters of polynomial (18) and then it is possible to write characteristic polynomial (20) as a combination of polynomial (18) and product root of factors in positive power of variable z

$$D_6(z) = \left(z^3 + a_{s1} z^2 + a_{s2} z + a_{s3}\right)(z-\lambda)(z-\mu)(z-\nu) \tag{21}$$

where λ, μ, ν are user-defined real poles. After modification (21) the characteristic polynomial is in the following form

$$D_6(z) = z^6 + d_1 z^5 + d_2 z^4 + d_3 z^3 + d_4 z^2 + d_5 z + d_6 \tag{22}$$

After comparison of (21) and (22) it is possible to obtain expressions for computation of individual parameters of polynomial (22)

$$\begin{aligned} d_1 &= a_{s1} - (\lambda + \mu + \nu) \\ d_2 &= a_{s2} - a_{s1}(\lambda + \mu + \nu) + \lambda\mu + \lambda\nu + \mu\nu \\ d_3 &= a_{s3} - a_{s2}(\lambda + \mu + \nu) - a_{s1}\nu(\lambda\mu + \lambda\nu + \mu\nu) - \lambda\mu\nu \\ d_4 &= -a_{s3}(\lambda + \mu + \nu) + a_{s2}(\lambda\mu + \lambda\nu + \mu\nu) - a_{s1}\lambda\mu\nu \\ d_5 &= a_{s3}(\lambda\mu + \lambda\nu + \mu\nu) - a_{s2}\lambda\mu\nu \\ d_6 &= -a_{s3}\lambda\mu\nu \end{aligned} \tag{23}$$

Then the 2DOF controller design consists of determination of parameters (23) of polynomial (22) using command (11) from the Polynomial Toolbox and solution of the Diophantine equation for computation of feedback controller parameters

$$A_s(z^{-1})K(z^{-1})P(z^{-1}) + B(z^{-1})Q(z^{-1}) = D_6(z^{-1}) \tag{24}$$

where

$$\begin{aligned} &K\left(z^{-1}\right) = 1 - z^{-1}; \quad P\left(z^{-1}\right) = 1 + p_1 z^{-1} + p_2 z^{-2}; \\ &Q\left(z^{-1}\right) = q_0 + q_1 z^{-1} + q_2 z^{-2} + q_3 z^{-3} \end{aligned} \tag{25}$$

and from expression (7).

The primary 2DOF controller output is given by

$$\begin{aligned} u(k) = {} & r_0 w(k) - q_0 y(k) - q_1 y(k-1) - q_2 y(k-2) \\ & + (p_1 - p_2) u(k-2) - p_2 u(k-3) \end{aligned} \tag{26}$$

where

$$r_0 = \frac{1 + d_1 + d_2 + d_3 + d_4 + d_5 + d_6}{b_1 + b_2} \tag{27}$$

IV. Simulation Verification and Results

A simulation verification of the designed control algorithms was performed in MATLAB/SIMULINK environment. The robustness of individual control loops was experimental investigated by a change of the static gain K of the nominal process model. From the point of view of the robust theory it is possible to consider these experiments on behalf of the gain margin determination by the parametric uncertainty influence.

The experimental process model was described by the second order continuous-time transfer function

$$G(s) = \frac{2}{(4s+1)(s+1)} e^{-8s} \tag{28}$$

The individual simulation experiments are realized subsequently: the static gain K was increased as far as the control closed-loop was in the stability boundary (no damping oscillation was achieved).

A. *Control Using Primary Controller (13)*

Let us now discretize (28) using a sampling period $T_0 = 2$ s. The discrete form of these transfer function is the nominal discrete model and it is expressed by

$$G_L\left(z^{-1}\right) = \frac{0.4728 z^{-1} + 0.2076 z^{-2}}{1 - 0.7419 z^{-1} + 0.0821 z^{-2}} z^{-4} \tag{29}$$

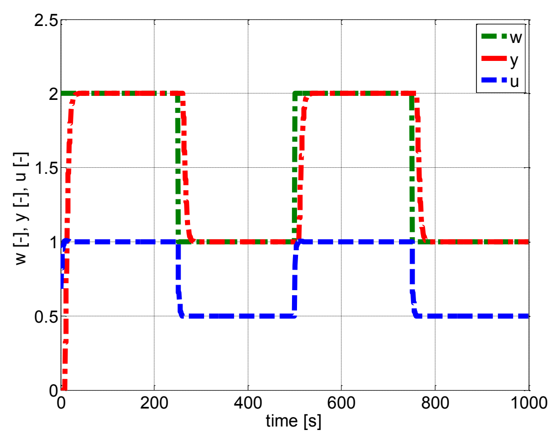

Fig. 3 Control of nominal model $G_L\left(z^{-1}\right)$, $K = 2$

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For all experiments the penalization factor was chosen as $q_u = 2$.

The characteristic polynomial $D_4(z)$ is given by

$$D_4(z) = z^4 - 1.1461z^3 + 0.4409z^2 - 0.00652z + 0.0032$$

with individual poles

$\alpha = 0.3796;\quad \beta = -0.7419;\quad \gamma = 0.1;\quad \lambda = 0.5$.

The control courses of the process output and controller output for the nominal model are shown in Fig. 3.

Perturbed models:

$$K = 3:\quad G_{P1}\left(z^{-1}\right) = \frac{0.7092z^{-1} + 0.3114z^{-2}}{1 - 0.7419z^{-1} + 0.0821z^{-2}} z^{-4} \tag{30}$$

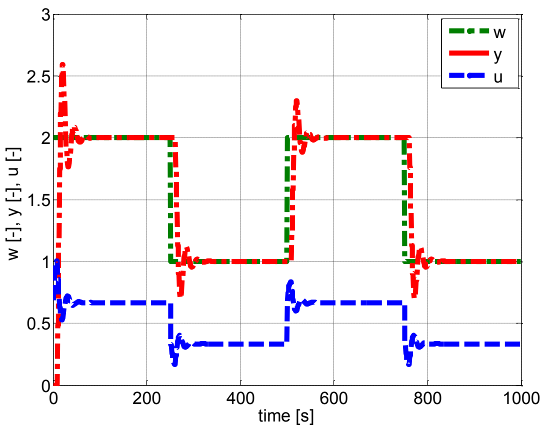

Fig. 4 Control of perturbed model $G_{P1}\left(z^{-1}\right)$, $K = 3$

$$K = 4:\quad G_{P2}\left(z^{-1}\right) = \frac{0.9456z^{-1} + 0.4153z^{-2}}{1 - 0.7419z^{-1} + 0.0821z^{-2}} z^{-4} \tag{31}$$

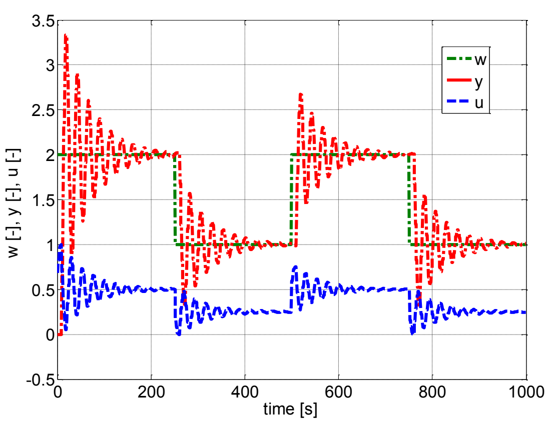

Fig. 5 Control of perturbed model $G_{P2}\left(z^{-1}\right)$, $K = 4$

$$K = 4.4:\quad G_{P3}\left(z^{-1}\right) = \frac{1.0402z^{-1} + 0.4568z^{-2}}{1 - 0.7419z^{-1} + 0.0821z^{-2}} z^{-4} \tag{32}$$

The control courses of the process output and controller output for the individual perturbed models are shown in Figs. 4 - 6. It is obvious from Fig. 6 that for the static gain $K = 4.4$ is the closed-loop control on the stability boundary. It is obvious from these Figs. that approximate interval of the robust stability of nominal model (31) is for the static gain $K = (2,\ 4.4)$.

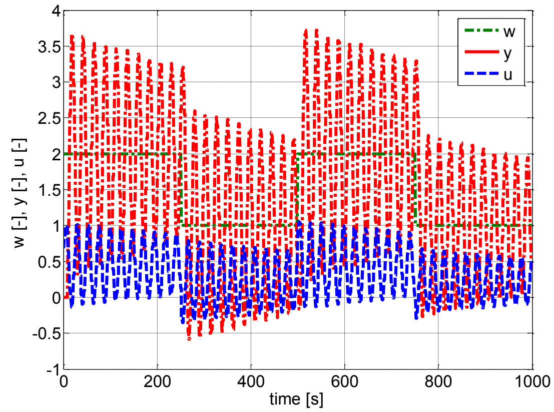

Fig. 6 Control of perturbed model $G_{P3}\left(z^{-1}\right)$, $K = 4.4$

B. *Control Using Primary Controller (29)*

Nominal discrete model (32) and penalization factor $q_u = 2$ was used for all simulation experiments; the characteristic polynomial $D_6(z)$ is given by

$$\begin{aligned} D_6(z) = {} & z^6 - 1.6438z^5 + 1.1466z^4 - 0.4052z^3 \\ & + 0.0743z^2 - 0.0067z + 2.2920e-04 \end{aligned} \tag{33}$$

with individual poles

$\alpha, \beta = 0.4561 \pm 0.2867i;\ \gamma = 0.1317;\ \lambda = 0.1;\ \mu = 0.2;\ \nu = 0.3$.

The control courses of the process output and controller output for the nominal model are shown in Fig. 7.

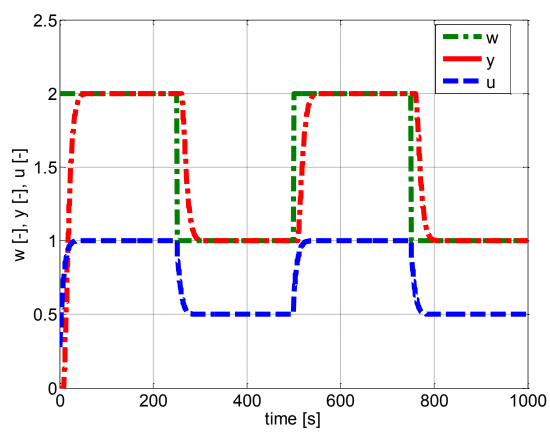

Fig. 7 Control of nominal model $G_{\Delta L}\left(z^{-1}\right)$, $K = 2$

The control courses of the process output and controller output for the individual perturbed models are shown in Figs. 8 - 10. It is obvious from Fig. 10 that for the static gain $K = 6.6$ is the control closed-loop on the stability boundary. It is obvious from these Figs. that approximate interval of the robust stability of nominal model (29) is for the static gain $K = (2,\ 6.6)$.

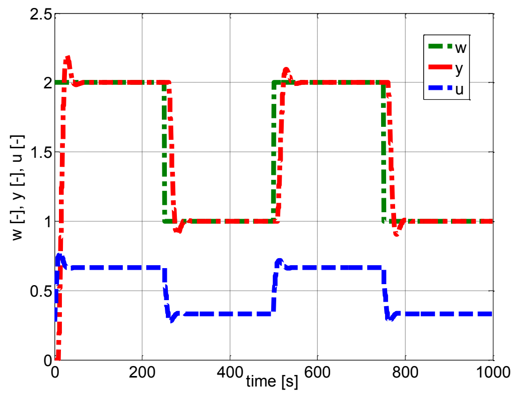

Fig. 8 Control of perturbed model $G_{\Delta P1}\left(z^{-1}\right)$ - $K = 3$

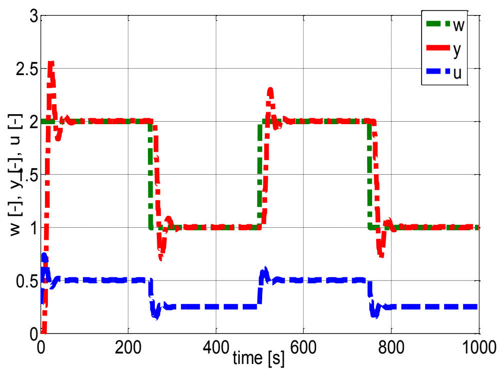

Fig. 9 Control of perturbed model $G_{\Delta P2}\left(z^{-1}\right)$ - $K = 4$

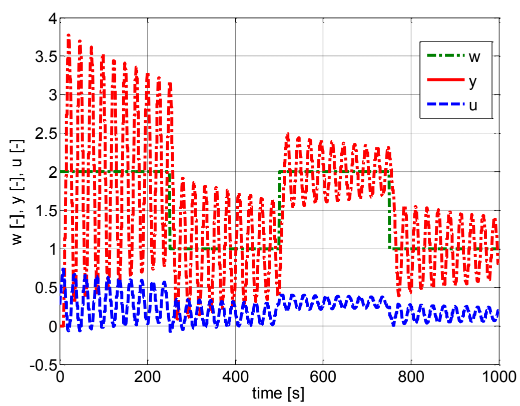

Fig. 10 Control of perturbed model $G_{\Delta P3}\left(z^{-1}\right)$ - $K = 6.6$

V. Conclusion

The paper presents an experimental simulation investigation of robust algorithms for control of time-delay systems. The MATLAB Polynomial Toolbox 3.0 is used for design of the polynomial digital Smith Predictor. The primary controllers of the digital Smith Predictor are based on minimization of the LQ criterion using spectral factorization. Two types of minimization of LQ criterions have been designed. In criterion (8) it is minimized a square of the controller output $u(k)$ – controller (13). In criterion (15) it is minimized a square of the increment value of the controller output $\Delta u(k)$ – controller (26). Simulation experiments demonstrated the influence of static gain K (parametric uncertainty) on the course of control variables (robustness of the control closed-loop). From comparison of both methods it is evident that minimization criterion (9) leads to faster courses of control variables. However the control-loop is in the stability boundary for a lower value K as in the case of minimization criterion (15). However minimization criterion (15) leads to quieter courses of control variables with their smaller oscillations for grater values of static gain K. The controller (26) is more conservative and robust than controller (15). The both control algorithms are relative simply and they are suitable for application in real-time conditions (see [20]).

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