Abstract—In this paper, a new voltage-mode MOS-C quadrature sinusoidal oscillator circuit based on composite second-generation current conveyor (CCCI) is presented. The proposed topology employs two CMOS based CCCI and four grounded components. CCCI is implemented by two CCII, so it also is possible to employ the circuit by commercially available AD844 by Analog Devices. The validity of the proposed circuit has been verified by PSPICE simulation programme. Simulation is done for both CMOS based implementation and AD844 based implementation of CCCI. It is seen that the simulation results agree well with the theoretical analysis and the proposed circuit achieves a good THD performance. The resistors used in the circuit are implemented by MOS transistors. So, the proposed circuit is fully integrable and it is possible to adjust the oscillation frequency by external MOS gate voltage. Also, it is stated how the CCCI employing circuit enhance the circuit performance when compared to the same topology employing CCII.

Keywords—Analog integrated circuits, Current conveyors, MOS-C realization, Oscillators.

I. INTRODUCTION

Quadrature sinusoidal oscillators find wide range of applications in telecommunication, signal processing, instrumentation, measurement and control systems and they can offer sinusoidal signals with 90° phase difference that is a requirement for some devices such as quadrature mixers, phase modulators and single-sideband generators [1]-[4]. For measurement purposes, quadrature sinusoidal oscillators are used as vector generators or selective voltmeters [5].

During recent years, several implementations of quadrature sinusoidal oscillators employing different high-performance active building blocks such as current feedback operational amplifier(CFOA), different types of current conveyor, four terminal floating nullor (FTFN), current follower, current differencing buffered amplifier (CDBA), current differencing transconductor amplifier (CDTA) and operational transresistance amplifier (OTRA) have been reported [6]-[21]. However, there is one or more drawbacks of these reported circuits such as excessive use of the passive elements, especially the external resistors, use of multiple-output active elements that makes the circuits more complicated, use of floating capacitor, which is not convenient for integration and the lack of electronic adjustment of the oscillation frequency.

The aim of this work is to present a new CCCI based quadrature sinusoidal oscillator realization and to do performance comparison to see how the CCCI based circuits have enhanced performance when compared to the same topology employing CCII. The features of the proposed circuit are as follows:

- The capacitors and resistors used in the circuit are all grounded.
- Resistors are implemented by MOS transistors, so the circuit is suitable for integration.
- Electronic adjustment of the oscillation frequency.
- Providing good characteristic with lower distortion than the oscillator circuit employing CCCI.
- Using only two active elements with single outputs.
- Possibility to adjust the oscillation frequency without affecting the oscillation condition.
- Possibility to employ the circuit by using commercially available AD844.

In the literature we have found, among the voltage mode quadrature sinusoidal oscillator circuits, none of them employs CCCI and have the whole features shown above.

II. CIRCUIT DESCRIPTION OF CCCI

The current conveyor is still emerging as one of the most important current-mode active building block and different types of current conveyor enable the researchers to design multipurpose circuits to be used in analog signal processing. CCCI can be constructed of two second generation current conveyors as shown in Fig.1 [22]. It is a useful technique to enhance the performance of the current conveyor by either lowering the x-terminal impedance or enhancing the y-terminal admittance [22]. This provides the CCCI based circuits have better output characteristics when compared to the same circuit topology employing CCII. In the CCCI-configuration, the lower conveyor CC2 works as a negative impedance conveyor and consequently the X-terminal impedance of the CCCI- is

\[ Z_{x(\text{composite})} = Z_{x1} + A_{12}Z_{x2} \cong Z_{x1} - Z_{x2} \]  

(1)

It is clearly seen from (1) that the current gain \( A_{12} \) should be designed slightly lower than the first in order to prevent a negative X-terminal impedance for the composite conveyor.

In addition, all even order nonlinearities in \( Z_{x1} \) and \( Z_{x2} \) are effectively summed together and hence X-terminal impedance nonlinearity is increased. Fortunately, in most cases the nonlinearity of the X-terminal impedance has little effect on the total amplifier distortion [22].

It is possible to implement the CCCI by using the current conveyor blocks as subcircuit. This current conveyor based CCCI implementation method makes it possible to employ the circuit by using commercially available AD844.

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III. PROPOSED CIRCUIT TOPOLOGY

The proposed CCCII based voltage-mode quadrature sinusoidal oscillator topology is shown in Fig. 2.

The circuit analysis of the proposed quadrature sinusoidal oscillator yields the following characteristic equation

\[ s^2 C_1 C_2 + G_1 G_2 = 0 \]  

The radian frequency of oscillation is

\[ \omega_0 = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \]  

The sensitivity of radian frequency to the passive components are all calculated as

\[ S_{R_1}^{\omega_0} = S_{R_2}^{\omega_0} = S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = -1/2 \]  

As it is shown in (4), the sensitivities of passive components are quite low.

IV. MOS-C REALIZATION OF THE PROPOSED CIRCUIT

A linear resistor has been realized by using parallel connection of two depletion type NMOS transistors operated in the triode region as illustrated in Fig. 3 [23]. This method cancels out the non-linearity of the MOSFET significantly.

Where \( W \) and \( L \) are the channel width and length and \( V_T \) is the threshold voltage of the MOSFET, \( \mu_n \) is the free electron mobility in the channel and \( C_{ox} \) is the gate oxide capacitance per unit area. The resistance values are tunable via \( V_C \) and since the even-order nonlinearities are cancelled out, it operates linearly over an extended voltage range. For achieving the fully MOS-C realization of the proposed oscillator circuit, the resistors must change with their MOS transistor conjugates.

Fig. 4 shows MOS-C realization of the proposed circuit. It is clear from this figure that the oscillation frequency of the circuit can be controlled by gate voltages \( V_{C1} \) and \( V_{C2} \) of the MOS transistors.

V. SIMULATION RESULTS

The proposed circuit’s performance has been evaluated for two different implementation of CCCII by PSPICE simulation programme using the MOSIS 0.35 μm CMOS process parameters and AD844 Macro-model parameters.

A. CMOS Based CCCII Simulation Results

The circuit schematic of CMOS CCCII used to implement the CCCII is shown in Fig. 5 [24]. The circuit is supplied with symmetrical voltages of ±1.25 V. W/L parameters of MOS transistors used in simulation are as in [24]. The biasing currents are taken as \( I_{B(CCCI+)} = I_{B(CCCI-)} = 5 \mu A \). The passive component values taken in simulation
are given in Table I. In the simulations, the process parameters of MOS transistors used to realize the resistors in Fig. 4, are taken as $W=8.3 \, \mu m$ and $L=0.7 \mu m$ for all M1, M2, M3 and M4. MOS gate voltages are taken as $V_{C1}=V_{C2}=2.9 \, V$ and the resistor value is found as $R \approx 254 \, \Omega$.

![Fig. 5 Circuit schematic of dual output CMOS CCII used for CCCII implementation](image)

**TABLE I. PASSIVE COMPONENT VALUES**

<table>
<thead>
<tr>
<th>$R_1$</th>
<th>$R_2$</th>
<th>$C_1$</th>
<th>$C_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>250 $\Omega$</td>
<td>250 $\Omega$</td>
<td>500 pF</td>
<td>500 pF</td>
</tr>
</tbody>
</table>

The calculated value of oscillation frequency is $f_0=1.27 \, MHz$. In order to make a performance comparison, two simulations are done for the circuits employing CCII and CCCII. The oscillation frequency and total harmonic distortion (THD) values obtained from the simulations are given in Table II. $V(1)$ and $V(2)$ denote the voltages across the capacitors $C_1$ and $C_2$.

**TABLE II. OSCILLATION FREQUENCY AND THD VALUES FOR CMOS IMPLEMENTATION**

<table>
<thead>
<tr>
<th>Oscillation Frequency (MHz)</th>
<th>Circuit employing CCII</th>
<th>Circuit employing CCCII</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.15</td>
<td>1.22</td>
<td></td>
</tr>
<tr>
<td>THD %</td>
<td>V(1) V(2)</td>
<td>V(1) V(2)</td>
</tr>
<tr>
<td>6.1</td>
<td>8.5</td>
<td>3.1 3.9</td>
</tr>
</tbody>
</table>

As it is seen from Table II, simulation results agree well with the theoretical calculations and the proposed circuit achieves a good THD performance. Table II also shows that the THD values of the circuit employing CCCII are significantly better than the values of the circuit employing CCII. The power dissipation of the circuit employing CCCII is 2.69 mW for the initial voltage of $0.2 \, mV$ given to $C_1$. The quadrature phase error is $1.98 \%$ and the oscillation frequency deviation error is $3.93 \%$ for the circuit employing CCCII.

In order to evaluate the tunability of oscillation frequency, the gate voltages of M2 and M4, which are shown as $V_{C1}$ and $V_{C2}$, are varied in a range of 2-3 V. The frequency values obtained by the variations of $V_{C1}$ and $V_{C2}$ are summarized in Table III.

**TABLE III. THE OSCILLATION FREQUENCY AND THD VALUES OBTAINED BY THE VARIATION OF $V_{C1}$ AND $V_{C2}$**

<table>
<thead>
<tr>
<th>$V_{C1}$, $V_{C2}$ (V)</th>
<th>Oscillation Frequency (MHz)</th>
<th>THD %</th>
<th>$V(1)$</th>
<th>$V(2)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.0</td>
<td>0.87</td>
<td>1.0</td>
<td>1.7</td>
<td></td>
</tr>
<tr>
<td>2.2</td>
<td>0.96</td>
<td>1.6</td>
<td>2.5</td>
<td></td>
</tr>
<tr>
<td>2.4</td>
<td>1.04</td>
<td>0.9</td>
<td>1.3</td>
<td></td>
</tr>
<tr>
<td>2.6</td>
<td>1.10</td>
<td>1.0</td>
<td>0.8</td>
<td></td>
</tr>
<tr>
<td>2.8</td>
<td>1.19</td>
<td>2.1</td>
<td>2.4</td>
<td></td>
</tr>
<tr>
<td>3.0</td>
<td>1.26</td>
<td>5.4</td>
<td>3.7</td>
<td></td>
</tr>
</tbody>
</table>

The voltage waveforms of the proposed circuit employing CMOS based CCCII are shown in Fig.6.

![Fig. 6 Simulation results of the quadrature sinusoidal oscillator circuit by using CMOS based CCCII. (a) Initial state waveform (b) Steady state waveform (c) The frequency spectrum](image)

B. AD844 Based CCCII Simulation Results

Another simulation is done by using the AD844 SPICE Macro-model parameters to check the workability of the presented circuit. The circuit is supplied with symmetrical $\pm 10 \, V$ and the passive component values taken in simulation are as shown Table I. As it is done before, two simulations are done for the circuits employing CCII and CCCII. The oscillation frequency and THD values obtained from the simulations are given in Table IV.

**TABLE IV. OSCILLATION FREQUENCY AND THD VALUES FOR AD844 IMPLEMENTATION**

<table>
<thead>
<tr>
<th>Oscillation Frequency (MHz)</th>
<th>Circuit employing CCII</th>
<th>Circuit employing CCCII</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.20</td>
<td>1.23</td>
<td></td>
</tr>
<tr>
<td>THD %</td>
<td>V(1) V(2)</td>
<td>V(1) V(2)</td>
</tr>
<tr>
<td>4.6</td>
<td>4.3</td>
<td>1.6 3.4</td>
</tr>
</tbody>
</table>

Also in AD844 based CCCII implementation, the THD values of the circuit are better than the values of the circuit employing CCII as shown in Table IV. The power dissipation of the circuit employing CCCII is 659 mW for the initial voltage of $0.1 \, mV$ given to $C_1$. The quadrature phase error is $0.64 \%$.

The voltage waveforms of the proposed circuit employing AD844 based CCCII are shown in Fig.7.
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Fig. 7 Simulation results of the quadrature sinusoidal oscillator circuit by using AD844 based CCCII. (a) Initial state waveform (b) Steady state waveform (c) The frequency spectrum

VI. CONCLUSION

A voltage-mode MOS-C quadrature sinusoidal oscillator based on CCCII has been presented. The resistors used in the circuit are implemented by MOS transistors and the capacitors are all grounded. So, the proposed circuit is fully integrable and it is possible to adjust the oscillation frequency by external MOS gate voltage. The simulation results agree well with the theoretical analysis. The proposed circuit achieves a good THD performance and the quadrature phase error is quite low. It is stated that the CCCII employing circuits enhance the circuit performance significantly when compared to the same topology employing CCII. The workability of the presented circuit is also verified by using commercially available AD844. It is expected that the proposed circuit will be useful in various telecommunication and signal processing applications.

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